WESTINGHOUSE ELECTRIC CORPORATION
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FINAL REPORT

CONTRACT NAS8-5335

June 1963 through October 1965

DESIGN, DEVELOP, FABRICATE AND DELIVER SILICON POWER TRANSISTORS

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama

ABSTRACT

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High power, high speed transistors were fabricated on large area epitaxial slices. The collector and the base regions were grown epitaxially and the emitter region was formed by diffusion. The transistors were hard soldered to moly and encapsulated using the compression bonding technique. The electrical characteristics of the transistor are:

collector to emitter voltage	V_{CEO} = 120 to 200 volts
current transfer ratio	h_{FE} = 10 to 15 at 100A
saturation voltage	$V_{CE(sat)}$ = .3 to 1.2 volts
turn-on time	t_{on} = 1 to 1.5μsec. at 20A
turn-off time	t_{off} = 0.4 to 0.7μsec. at 20A

thermal impedance = 0.2 to 0.35°C/watt.

Proven is the feasibility of fabricating high voltage, high current, and high speed devices on large area epitaxial slices.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS
(cont'd.)

I. INTRODUCTION

A. REVIEW OF SPECIFICATION

Work was started at Westinghouse Semiconductor Division in August 1964 to design, develop, fabricate and deliver silicon power transistors for NASA under Contract NAS8-5335. The electrical, thermal and environmental specifications of the transistor are given below.

1. Electrical

a. DC current transfer ratio, h_{FE} minimum 10 at 100 amperes DC at r_{CES} = .010 ohms maximum.

b. Collector to emitter voltage: V_{CEO} = 150 volts minimum.

c. Collector current at V_{CE} = 200 volts, T_j = 200°C, V_{EB} = -1.5V: 30ma.

d. Emitter current at V_{EB} = 10 volts, T_j = 200°C, I_C = 0. Maximum I_{EBO} = 25ma.

e. Base voltage at I_C = 100 amperes, I_B = 10 amperes, $V_{BE(sat)}$ = 2.5 volts maximum.

f. Turn-on time at I_C = 100 amperes, I_B = 10 amperes, V_{CE} = 12 volts, $t_d + t_r$ = 1.0 microseconds maximum.

g. Turn-off time at V_{BE} = -5 volts, V_{CE} = 12 volts, $t_s + t_f$ = 3.0 microseconds maximum.

2. Thermal

Collector power dissipation, P_C, watts	- 250
Thermal resistance, O_{J-C}, °C/watt, max.	- 0.45
Typical thermal capacitance, C_t, watt-sec/°C	- 0.6
Typical thermal time constant, T_{J-C}, milliseconds	- 120

3. Environmental

a. Temperature cycling: -65°C to +200°C, 5 cycles

b. Moisture resistance: 10 cycles

c. Centrifugal: 500g

d. Storage life: +200°C, 1000 hours

e. Shock: 500g

f. Vibration: 20g, 100cps to 2000cps

B. MAJOR DIFFICULTIES ENCOUNTERED

The transistor was first designed to be fabricated on an epitaxially grown collector region with a diffused base and a diffused emitter. In this design 19, 10-ampere transistors were fabricated on 1-inch diameter slices. The encapsulation of these 19 transistors to produce a total 100-ampere unit was found to be extremely difficult. Consequently, the emitter geometry was changed and a single 100-ampere transistor was fabricated on a 1-inch diameter slice. The impurity profile in this case also was a double diffused single epitaxial profile. The leakage of the transistors fabricated according to this design was found to be very high. In order to locate the leakage problem, one slice from each group was taken and a 10-ampere control transistor was fabricated along with a large 100-ampere transistor. Each control slice contained 19 small units. About 25% of the small 10-ampere transistors showed poor voltage capability while the remaining 75% showed fairly good voltage and high leakage. This investigation apparently indicated that the low voltage and high leakage were either due to the nonuniform quality of the epitaxial layer over a large area or due to the impurities introduced during the diffusion process.

In the third phase of this program, it was decided to introduce techniques to improve the quality of the epitaxial growth and also to change the impurity profile to a double epitaxial single diffused one. This design

showed very promising results and the final transistors were fabricated accordingly.

The formation of the collector-base junction by mesa etching instead of sandblasting was found to be better from a leakage standpoint. This was so because the etchant used to etch the junction after sandblasting reacted with the hard-soldering alloy and the moly. This in turn contaminated the junction. Mesa etching a groove 10 microns deep eliminated this contamination and improved the leakage.

During the fourth phase of the program, the modifications were introduced in the encapsulation system and also in the mounting of the transistor to moly. The transistor was designed to be encapsulated with a compression bonding technique. A silver ring was used as the emitter contact. With the application of pressure on the order of 1200 lbs. the silver ring was found to flatten and short the emitter-base contact. It was found that the units were cracking on the application of high pressure. The design of the emitter contact was changed to a silver foil wrapped around a Teflon disc which gave a satisfactory contacting system.

Difficulties were also encountered in mounting the transistor to the moly. Usually after putting on the aluminum contact, the collector side of the transistor was evaporated with gold and hard soldered to gold plated moly. This step was found to produce a degradation in voltage and gain. This degradation was eliminated by hard soldering the transistors straight to the plain moly using a rectifier-type solder.

Thus the difficulties encountered in connection with epitaxial material preparation, fabrication, mounting and encapsulation were successfully eliminated and the program was completed according to the specifications of the subject contract.

C. MAJOR ACCOMPLISHMENTS

The successful completion of the project demonstrated the following important factors:

1. The formation of a defect-free epitaxial junction over a large area was possible. This was demonstrated by the uniformity in the breakdown voltage and also by the low leakage of the epitaxial junctions.

2. The value of in situ deposition of the collector-base junction. This technique virtually eliminated the damage introduced due to handling or exposure to a contaminating atmosphere.

3. That tight control over the emitter diffusion process and the photo masking technique was possible. The good characteristics of the final device was evidence of success.

4. The fabrication of high speed (4μs), high current (100A), high voltage (150V) and low saturation voltage transistors on large area epitaxial slices is possible.

5. A method of encapsulation giving low thermal impedance (0.35°C/watt). This was mainly due to the well controlled compression bonding technique. This technique helped to eliminate serious soldering problems such as thermal fatigue or degrading of device characteristics due to voids.

II. DESIGN CONSIDERATIONS

A. INTRODUCTION

The device specified under this contract is outstanding in its rating of current, voltage, switching time and saturation characteristics.

The high voltage requirement is usually not compatible with narrow base widths since the collector voltage will either be punch-through or multiplication limited if the base doping is too low or too high, respectively. Studies in secondary breakdown and negative resistance in collector characteristics are described. The $\alpha M = 1$ condition is shown to be affected by the emitter geometry and to dominate the SB phenomena. It is fortunate that the requirement on α control is similar to that required for switching time. With the α already under control, the collector junction is then designed for a predetermined multiplication factor, $M = 1/\alpha$, that permits the use of a small base width required for fast switching. The voltage capability of the device can be determined by establishing the dependence of breakdown voltage on the various device parameters.

Using the theory based on Moll's[1] work, the switching time characteristics can be analyzed. It is shown that if the transistor gain is controlled and maintained relatively constant throughout the operating range of current and temperature, the fall and rise times can be minimized.

Of the three components of transistor current gain (emitter efficiency, transport efficiency, collector efficiency), it is usually the emitter efficiency that determines the current gain of present day silicon transistors. In general, emitter efficiency and current gain tend to increase with emitter current as recombination consumes less of the injected current, and to decrease at high current levels due to an

(1) Moll, J. T., "Large Single Transient Response of Junction Transistors," Proc. IRE, V. 42, pp. 1773-1784, Dec. 1954.

effective increase of carrier concentration in the base (conductivity modulation). These effects combine to give a gain characteristic which is low at very low current, rises to a maximum at moderate currents, and falls off at high currents. Gain at very high current is determined largely by emitter edge length, since the transverse voltage drop across the base region leads to crowding of current to the emitter edges.[3] For the best utilization of total device area at high currents, the ratio of emitter edge length to emitter area must be reasonably large. Westinghouse power transistor designs employ multiple ring structures for this purpose. Other means of achieving this end in the industry include interdigitated or comb structures and various types of star structures. Theory and experience both indicate that the current density per unit of emitter edge length should be on the order of 4-5 amperes per inch. Thus, the subject 100-ampere transistor will require some 20-25 inches of emitter edge.

To reduce gain falloff due to conductivity modulation, in the first place, a highly doped base region is required. In order to achieve the 200-volt collector-emitter rating, either the collector region must be lightly doped, or the base region must include a high-resistivity layer adjacent to the collector junction. The general device structure must therefore be of either the $N^+P^+\pi N^+$ or $N^+P^+VN^+$ type, where π and V denote high resistivity P and N types, respectively. Of these, the $N^+P^+VN^+$ structure would give the lower variation of current gain with collector voltage. The collector contact region is N^+ (that is, highly doped) in both cases to minimize collector body resistance in order to keep saturation resistance and collector charge storage low.

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(2) Webster, W. M., "On the Variation of Junction-Transistor Current-Application Factor with Emitter Current," Proc. of IRE, V. 42, pp. 914-920, June 1954.

(3) Fletcher, N. H., "Some Aspects of the Design of Power Transistors," Proc. of IRE, V. 43, pp. 551-559, May 1955.

Further control of gain at low and moderate currents can be achieved by suitable design of the overall emitter area and of emitter doping level, particularly since the base doping is already increased. By increasing the total emitter area, recombination is made a dominant factor up to higher emitter currents; in this way, the peak of the gain curve is lowered in magnitude and shifted to higher current levels. The gain falloff is thus reduced and saturation voltage is also minimized. The total emitter area should therefore be as large as physical limitations and switching time considerations permit.

The fundamental emitter efficiency can be controlled by the emitter doping level or, in the case of a diffused emitter, by the relative depth of diffusion and the surface concentration, as is well known to the industry. In the subject device, the emitter efficiency will be controlled to the lowest level compatible with gain requirements; i.e., the doping level in the emitter will be high enough to achieve the desired gain, but no higher.

In this section the design equations used to compute the voltage capability, current gain and switching characteristics are given and the emitter geometry is discussed.

B. EMITTER GEOMETRY

Initially a novel design approach was considered which would take into consideration any defects formed in the crystal structure during fabrication, such as pipes and spikes, which would limit the performance of the device. The approach under investigation called for a series of individual emitters formed by oxide masking and diffusion on a single crystal. Only those emitters found to be in specification would be connected externally in order to meet the current gain and voltage requirements. Use of individual emitters on the silicon would allow considerably greater effective emitter edge length to be obtained in a given area than in the conventional interdigitated comb structure where area must be used for emitter interconnections.

The individual emitters were to be strips formed by diffusion into silicon, each strip being 10 mils in width separated by a base strip of 5 mils width. The total emitter edge length, when strips of this size are employed, would be 42 inches.

Unfortunately, problems of encapsulation made it necessary to abandon this initial approach. Tolerances involved in using a ceramic disc to make contact to the emitter and base area of the silicon device were too fine; and the orientation of the ceramic disc within the case was nearly impossible. These technological difficulties offset any advantages that may have accrued using this design.

Another method employing the redundancy concept was developed. In this approach a series of 10 ampere modules was fabricated on a single silicon slice incorporating the original diffusion profiles, oxide masking and photo-resist techniques. The best of these modules were connected in parallel to obtain 100 amperes. Each module is a separate transistor isolated from the other transistors on the slice by mesa etching. A

hexagonal shape was chosen for each module. This shape had the advantage of filling the surface of a circular slice of silicon with very little waste. In addition, the opposing apexes of the hexagon offered suitable areas for contacting the base and emitter of each module.

Nineteen modules could be placed on a slice 1 1/8 inch in diameter in the manner pictured in Figure 1 . Each module has an emitter with an edge length of approximately 2.5 inches, as required for 10 ampere operation. The total array is therefore theoretically capable of operating at 190 amps. This redundancy design offers advantages in fabrication yield, gain, and saturation characteristics for the subject transistor. The detailed dimensions of the emitter mask are shown in Figure 2.

Since potential problems in interconnection were foreseen, a conventional non-redundant design was developed simultaneously.

In a review with NASA of device requirements it was determined that the case outline that had been considered was too large. To accommodate the smaller case size, the slice size was reduced from 1 1/8 inches to 1 inch. With this overall size reduction, the original concept of 19 modules was retained by reducing the size of each module to 80% of that previously considered. The emitter edge length per module then became 2.0 inches, requiring a current density of 5 amperes/inch.

Difficulties were encountered in interconnection and encapsulation of the nineteen module units. Due to this problem, a single 100 amp unit was designed. This is the design employed in the final transistor and the dimensions are shown in Figure 3 . The design consists of forty-five emitter fingers with a total emitter edge length equal to 21 inches and a total emitter contact area equal to 0.5 $(in.)^2$.

C. VOLTAGE DESIGN

A complete knowledge of avalanche breakdown characteristics and also the depletion layer properties is essential for the optimum voltage design of transistors. The steps that have to be taken for voltage design are the determination of the net impurity distribution across the device and the solution of the Poisson's equations for the appropriate boundary conditions. The design of multi-diffused transistors is much more complicated than single-diffused or alloy transistors. This is mainly due to the fact that multi-diffused structures introduce several design parameters whose interdependence is hard to investigate. A detailed analysis has been made at Westinghouse with the aid of IBM-7094 computer to determine avalanche breakdown voltage and the voltage supported by the collector-base junction for the given values of:

(1) depletion layer width
(2) surface concentration
(3) background concentration of the parent material
(4) diffusion depths.

The net impurity density for a Gaussian distribution in the region AB (see Figure 4) is

$$C(x) = C_1 e^{-X^2/4D_1t_1} - C_2 e^{-X^2/4D_2t_2} + C_B \qquad (1)$$

where C_1 = surface concentration of emitter diffusion
C_2 = surface concentration of base diffusion
C_B = background concentration
D_1 = diffusion coefficient of the diffusant used for emitter diffusion
t_1 = emitter diffusion time
D_2 = diffusion coefficient of the diffusant used for base diffusion
t_2 = base diffusion time

The diffusion profile in the region BC for a Gaussian distribution is

$$C(x) = C_3 \; e^{-X^2/4D_3t_3} + C_B$$

where C_3 = surface concentration for collector diffusion
D_3 = diffusion coefficient for collector diffusion
t_3 = diffusion time

The Poisson's equation corresponding to the distribution given in Equation (1) is

$$\frac{d^2V}{dx2} = -\frac{qC(x)}{K\varepsilon_o} \qquad (2)$$

where q = electronic charge
K = dielectric constant
ε_o = permittivity of free space

The voltage capability of the collector-base junction can be calculated by solving Equation (2) for given boundary conditions.

When a voltage is applied at a junction, the depletion layer extends to both sides of the junction. The depletion layer width as a function of voltage at the collector base junction can also be calculated by solving Equation (2) for given boundary conditions.

The avalanche breakdown characteristics can be calculated from the empirical formula[4]

$$1 - \frac{1}{M} = \int_o^w \alpha\,(E)\,dx \qquad (3)$$

where M = avalanche multiplication factor
w = depletion layer width

The ionization rate can be written[5] as

$$\alpha\,(E) = a\; e^{-b/E}$$

(4) Muller, S. L., "Avalanche Breakdown in Germanium," Physical Review, V. 99, pp. 1234-1241, August 1955.
(5) Masergian, J., "Determination of Avalanche Breakdown P-N Junctions," J. of Appl. Physics, V. 30, pp. 1613-1614, October 1959.

where $a = 9 \times 10^{15}\ cm^{-1}$

$b = 1.7 \times 10^{6}$ (volt/cm)

The junction breaks down in the avalanche mode when the integral in Equation (3) becomes unity.

The results of the calculations pertinent to the subject transistor are shown in Table I. It is seen from Table I that Case I and Case II will meet the voltage requirement and that a collector region of 40μ and 17μ is needed for these two cases respectively. However, Case II has a definite advantage over Case I, since a thinner collector region will reduce the saturation resistance considerably. Thus, the parameters chosen for the basic design are:

Surface concentration for emitter diffusion:

$$C_1\ (atoms/cm^3) = 1 \times 10^{21}$$

Surface concentration for base diffusion:

$$C_2\ (atoms/cm^3) = 1 \times 10^{18}$$

Concentration for the intrinsic collector region:

$$C_B\ (atoms/cm^3) = 6.5 \times 10^{14}$$

Base diffusion depth:

$$X_{J_2}\ (microns) = 5$$

Base width:

$$W_B\ (microns) = 2{:}5$$

Problems were solved for the set of parameters shown in Table II and the results were analyzed graphically. A typical set of results is shown in Figure 5.

D. CURRENT GAIN

The current gain of a transistor can be written as

$$\alpha = \gamma \beta$$

assuming a collector efficiency of unity, where

γ = emitter efficiency
β = base transport factor

The current transfer ratio is

$$h_{FE} = \frac{\alpha}{1 - \alpha}$$

For transistors with fairly narrow basewidth, the transport factor is close to unity and, hence, the factor that influences most of the current gain is the injection efficiency γ . In the case of diffused transistors γ is mainly determined by surface concentrations, diffusion depths, lifetime of the minority carriers, and the drift-field intensity. The dependence of γ on these parameters can be determined by solving the steady state continuity equation for known boundary conditions. This analysis has also been done at Westinghouse with the aid of another computer program. The program computes the injection efficiency, the transport factor and current transfer ratio for given values of surface

concentrations, diffusion length and junction depths, taking into consideration the effect due to drift field also. At low-level injection the drift field is due to built-in concentration gradient, and at high-level the drift field is mainly due to the injected carriers.

The steady state continuity equation is

$$(q - R) - \nabla \cdot I = 0 \qquad (4)$$

(q-R) = net rate of generation of particles
(rate of generation - rate of recombination)

I = particle current.

The electron current due to diffusion and drift field in a P-type base is

$$I_N = - D_n \nabla N - \mu NE \qquad (5)$$

where N = excess minority carrier (electron density)

E = electric field intensity.

It can be assumed that

$$R = \frac{N}{\tau_n}, \quad q = 0 \qquad (6)$$

where τ_n = the lifetime of minority carriers.

Substituting equation (5) and (6) in (4), we get the steady state continuity equation for excess minority carrier in P-type base as

$$\frac{d^2N}{dx^2} + f \frac{dN}{dx} - \frac{N}{L_n 2} = 0 \qquad (7)$$

where $L_n 2 = \frac{1}{D_n \tau_n}$, $f = \frac{qE}{KT}$

The general solution of Equation (7) is

$$N = e^{- fx/2} \left[A e^{\alpha x} + B e^{-\alpha x} \right] \qquad (8)$$

where

$$\alpha^2 = \frac{f^2}{4} + \frac{1}{L_n^2}$$

The excess minority carrier current density is

$$J_N = -q\, I_N = q\, D_n \frac{dN}{dx} + q\, \mu_n\, NE \qquad (9)$$

The coefficient in Equation (8) can be evaluated with known boundary conditions at the edge of the depletion layer of the model shown in Figure 8 and current density can be determined from Equation (9). A similar type of equation can be derived for the minority carrier density J_P in the N-type emitter.

Thus, the injection efficiency of the emitter base junction is

$$\gamma = \frac{J_{N(X_2)}}{J_{N(X_2)} + J_{P(X_1)}}$$

and the transport factor is

$$\beta = \frac{J_{N(X_3)}}{J_{N(X_2)}}$$

and the current gain is

$$\alpha = \gamma\, \beta$$

assuming a collector efficiency of unity. Thus, the current transfer ratio

$$h_{FE} = \frac{\alpha}{1 - \alpha}$$

The above treatment can also be extended to PNP transistors. A series of problems were solved for the parameters given in Table II and the results were analyzed graphically.

E. SATURATION VOLTAGE

One of the critical design requirements of the subject transistor is for the low saturation voltage (1 volt) at a collector current of 100 amperes. In order to begin the design, it is necessary to examine the characteristics of a transistor operating under saturation conditions. The peculiar requirements placed on such a transistor will be considered in detail. A transistor in a typical common emitter circuit is shown in Figure 6 . Ordinarily, the collector junction, J_C, is reverse biased and the emitter junction, J_e, is forward biased by the supply voltages as shown. As the base current, I_B, is increased, the collector current, I_C, will also increase. However, if I_C is increased to the point where the $I_C R_L$ drop equals the E_{CC} supply voltage, the J_C is no longer reverse biased but forward biased as shown by the polarity marks. Thus, the saturation voltage, V_{CE}, is the difference between the collector junction voltage and the emitter junction voltage plus the ohmic drops across the collector, emitter and base region. The ohmic drops can be made small by high doping of these regions. Thus, the important point now is to make the collector and emitter junction voltages equal so the difference between them is small and thus V_{CE} is small.

The voltage drop across any junction is determined by the carrier density on each side of it. In a transistor with collector and emitter junctions adjacent to each other, this voltage is related to the normal and inverted alphas as given by Ebers and Moll[6]. Thus, making the collector and emitter junction voltages equal, requires equal doping in the emitter and collector regions. It is also essential to have a small base width so that the injected carrier density recombination loss from the emitter is small and almost the same at the collector. This is the same as keeping the base current small so that the collector and emitter currents are almost equal.

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(6) Ebers and Moll, PIRE V. 42, p. 1761, Dec. 1954.

A second requirement for a low saturation voltage becomes evident when the equivalent circuit of an ordinary transistor with collector-base contacts overlap is examined. The equivalent circuit and the overlap are shown in Figure 7 .

When V_{CC} in Figure 7 is less than V_{BE} minus the forward drop of the diode D, diode D will start to conduct and the current will start to flow through diode D. Thus, the external base current, I_{BT}, is no longer the only true base current, I_B, and an increase in V_{BE} in this mode will only pass more current through the diode. Thus, I_C is not affected by this action since only I_B can change I_C. The saturation voltage cannot be decreased further and thus V_{CE} is essentially clamped to V_{BE}.(7)

It is obvious that the voltage drop across R_{bb}' increases the saturation voltage if the impedance in the diode branch is low.

In summary, the above discussion indicates that this diode effect will be minimized if R_{bb}' is eliminated and/or the diode equivalent drop is increased. At the same time, the forward and inverse alphas should be maximized. This requires heavy symmetrical doping for emitter and collector and a narrow but sufficiently highly-doped base region. **The profile shown in Figure 8 approximately satisfies these requirements.**

F. SWITCHING CHARACTERISTICS

The parameters of switching time for a transistor in the common-emitter configuration as given by Moll(1) using a simplified equivalent circuit of a transistor are:

$$\text{Rise Time:} \quad t_o = \frac{1}{W_N(1-\alpha_{NO})} \ln \frac{1}{i_{B1} - 0.9\, i_{C1}\frac{\alpha_{NO}}{\alpha_{NO}}}$$

(7)H. G. Rudenberg,PIRE, p. 1304, June 1958.

$$\text{Storage Time:} \quad t_1 = \frac{W_N + W_1}{W_N W_1 (1-\alpha_{NO}\alpha_{10})} \ln \frac{i_{B2} - i_{B1}}{i_{B2} - i_{C1} \frac{1-\alpha_{NO}}{\alpha_{NO}}}$$

$$\text{Fall Time:} \quad t_2 = \frac{1}{W_N(1-\alpha_{NO})} \ln \frac{C1 - \frac{\alpha_{NO}}{1-\alpha_{NO}} i_{B2}}{0.1 i_{C1} - \frac{\alpha_{NO}}{1\alpha_{NO}} i_{B2}}$$

where

W_N = angular alpha cut-off frequency

α_{NO} = low frequency common base current gain

α_{10} = low frequency inverted common-base current gain

W_1 = angular cut-off frequency of α_1

i_{B1} = turn-on base drive

i_{B2} = turn-off base drive

i_{C1} = collector current in "on" state

In using the above equations, we assume that α_N, α_1, W_N, and W_1 do not vary with collector current **or** with voltage; and effects of emitter and collector capacitance are neglected.

If α increases appreciably from its minimum value (i.e. at 100 amperes for the subject device) in the range of current being switched, rise and fall times will increase. Therefore, a basic requirement for this transistor was a controlled gain characteristic with minimum variation of gain with current level. The calculated **rise** time of 0.4 microseconds indicates that a base width of 3-4 microns gives a conservative design for speed, leaving room for increases in switching time due to gain variation and capacitance effects. Furthermore, this base width leaves an adequate margin over the voltage-limited base width of 1.25 microns.

TABLE I

Results of Computer Calculations

Case	C_1 (atoms/cm^3)	C_2 (atoms/cm^3)	C_B (atoms/cm^3)	X_{J2} (μ)	W_B (μ)	A_1 (μ) at V=180V	V_{PT} (volts)	V_{AB} (volts)
I	10^{21}	10^{18}	1.5×10^{14}	5	2.5	40	1000	650
II	10^{21}	10^{18}	6.5×10^{14}	5	2.5	17	600	180

TABLE II

Sets of Parameters Used for Computer Calculations

C_1 (atoms/cm^3)	C_2 (atoms/cm^3)	C_B (atoms/cm^3)	$X_{j2}(\mu)$ Base Diff. Depth	$W_B(\mu)$ (base width)
1×10^{20}	1×10^{17}	1.5×10^{14}	4 -------->*	1.5, 2.5
1×10^{21}	1×10^{18}	6.5×10^{14}	5 -------->	1.5, 2.5, 3.5
	1×10^{19}	1.5×10^{15}		
		6.5×10^{15}	7 -------->	2.5, 3.5, 4.5, 5.5
			9 -------->	2.5, 3.5, 4.5, 6.5

* The double bracket and arrow indicate the combination of X_{j2} and W_B chosen for each run.

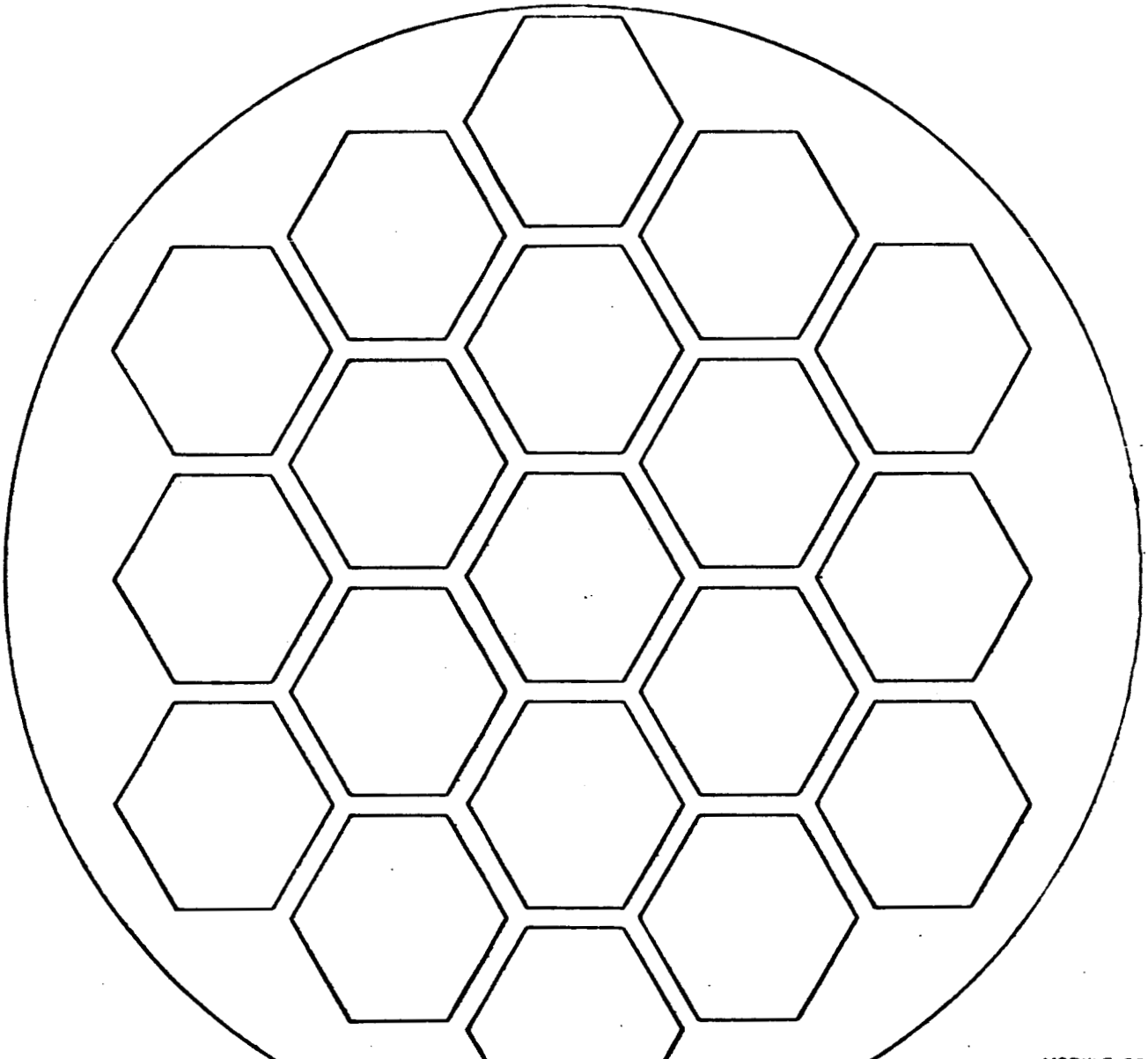


Figure 1

Nineteen Module Design

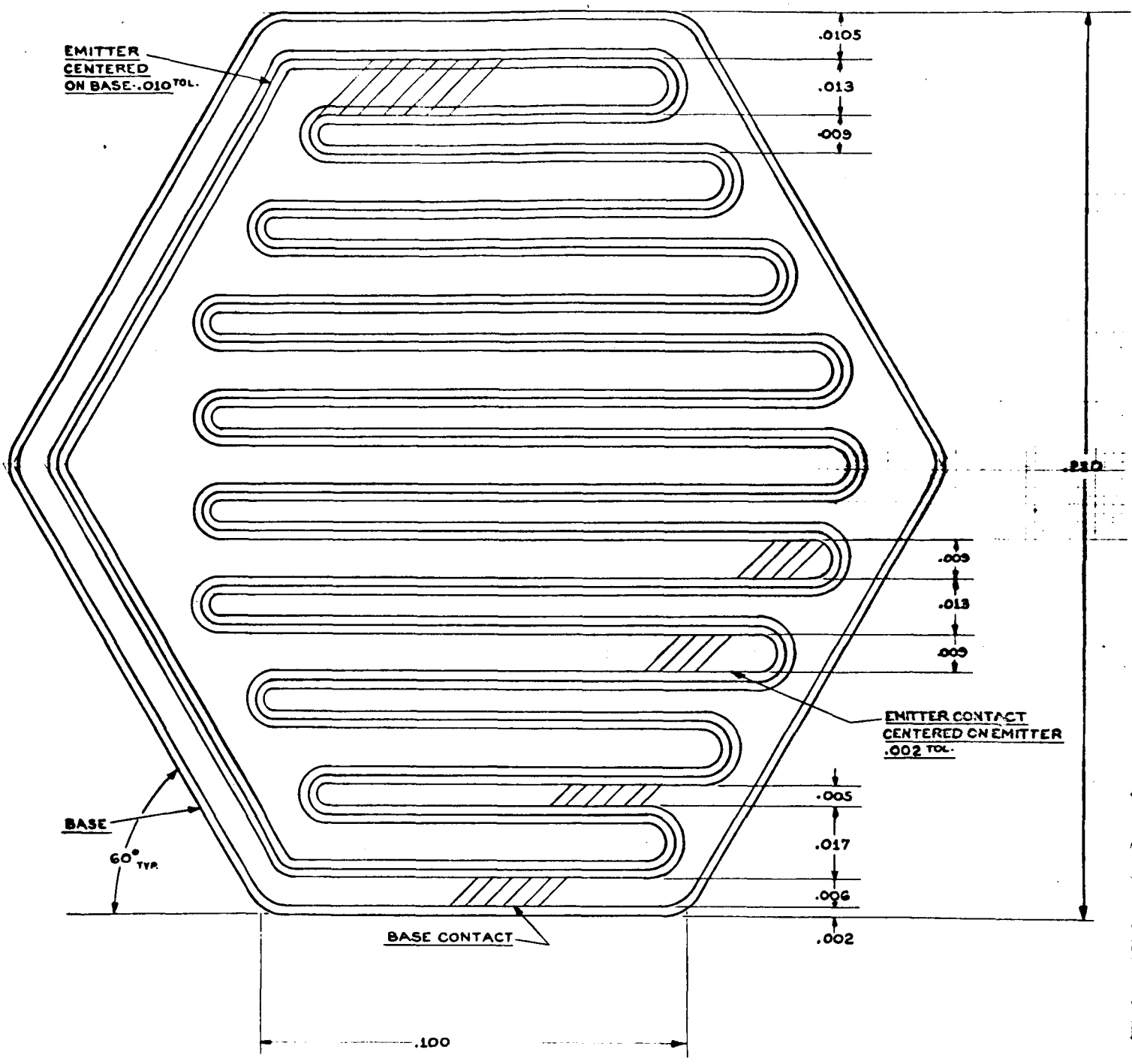


Figure 2

Detailed Dimensions of Emitter Mask for 19-Module Design

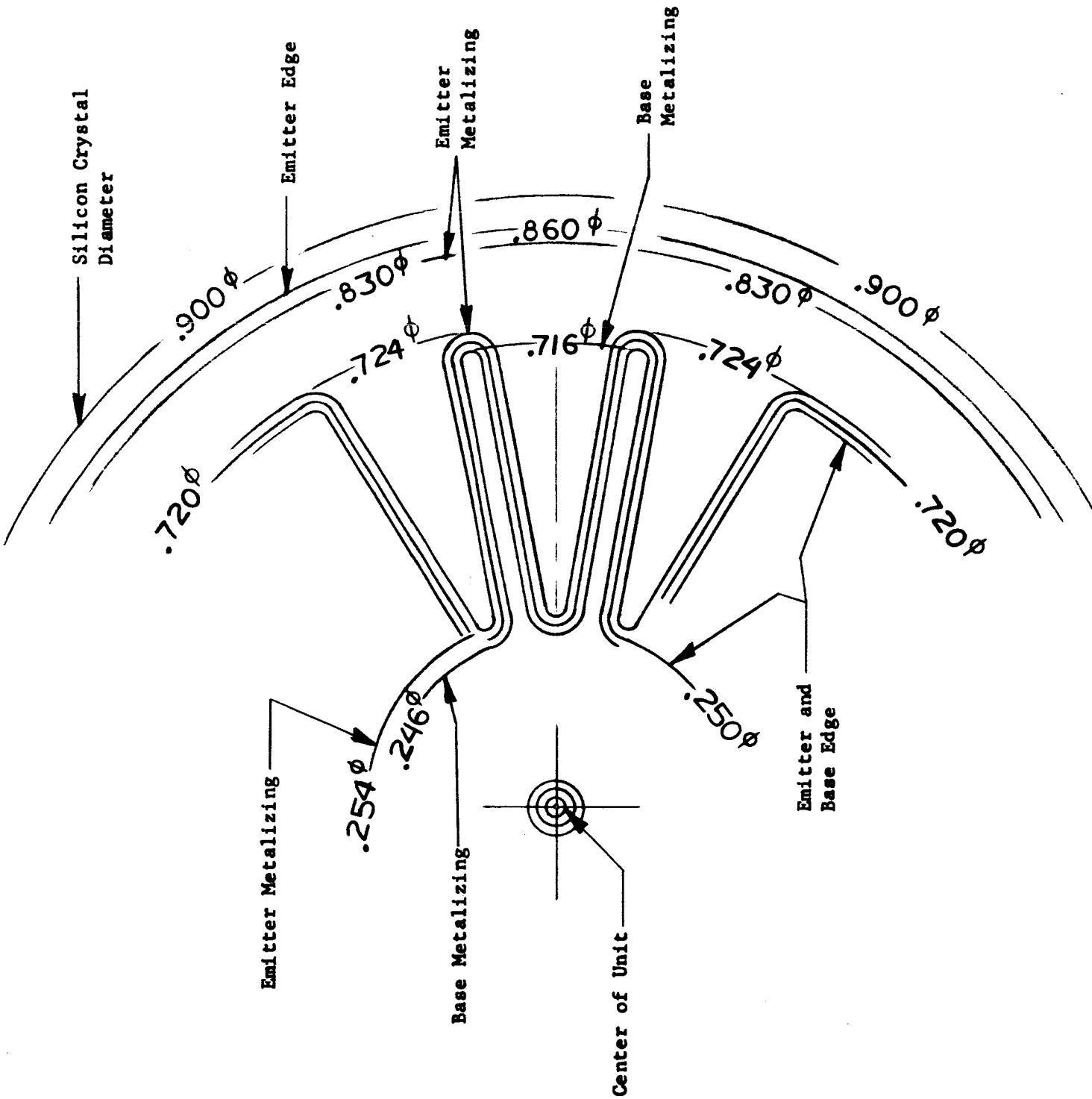


Figure 3

100 AMP TRANSISTOR

Final Design

$C_1 = 1 \times 10^{21}$ $X_{J1} = 3\mu$

$C_2 = 1 \times 10^{18}$ $X_{J2} = 8\mu$

$C_3 = 1 \times 10^{20}$ $X_{J3} = 50\mu$

$C_B = 1 \times 10^{14}$ $W = 10\mu$

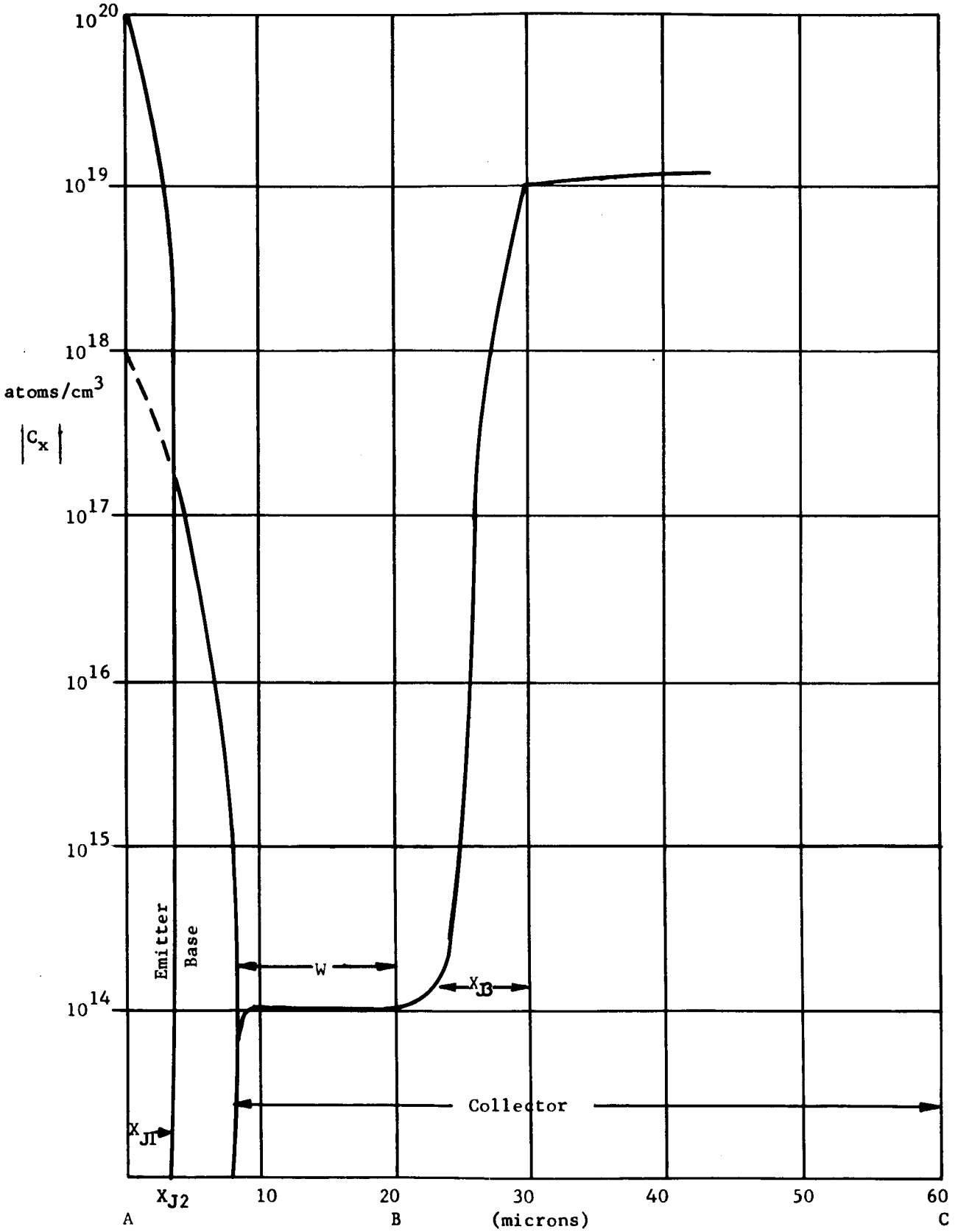


Figure 4: Net Impurity Density for a Gaussian Distribution

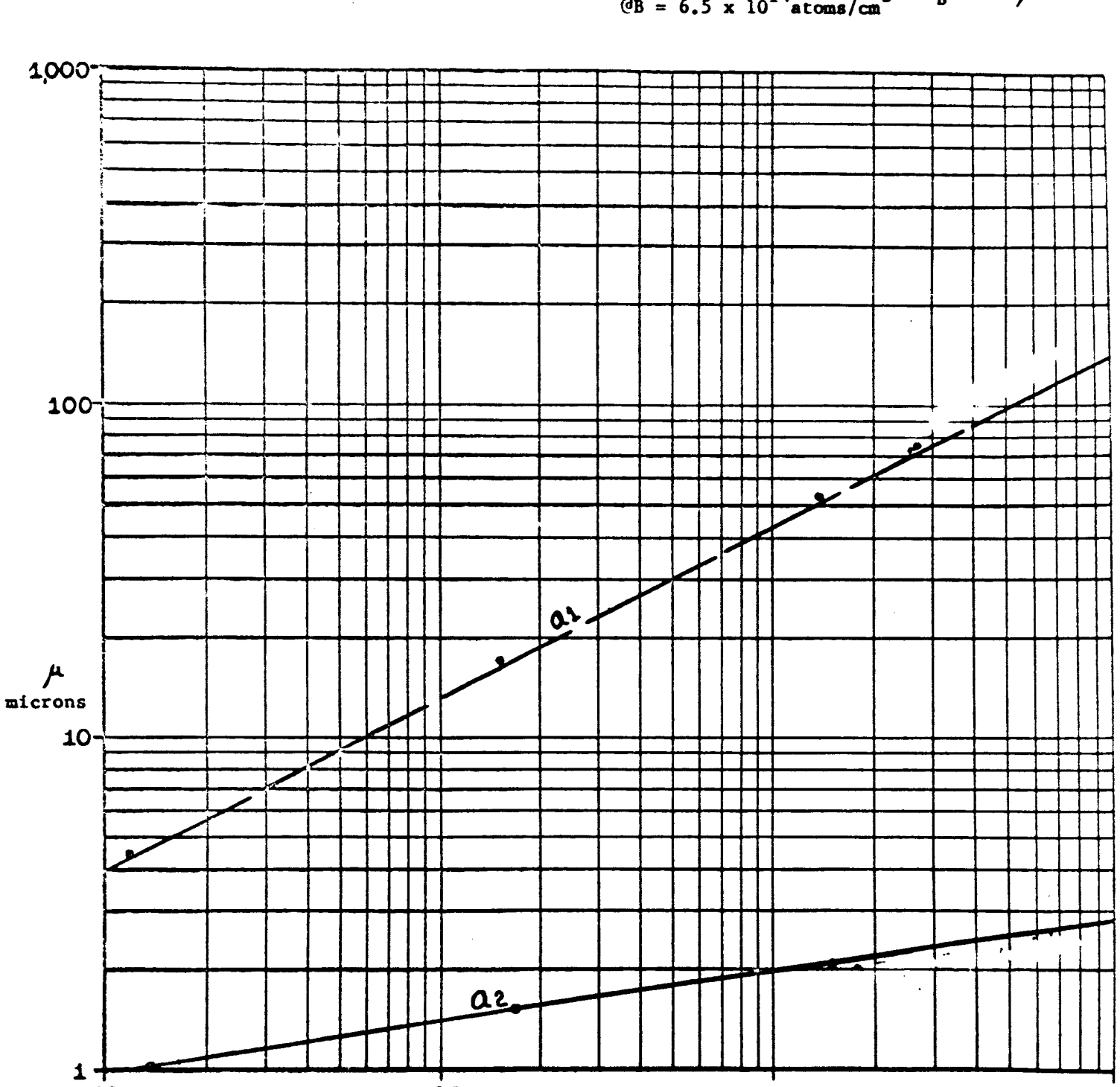


Figure 5

Typical Results of Computer Calculations

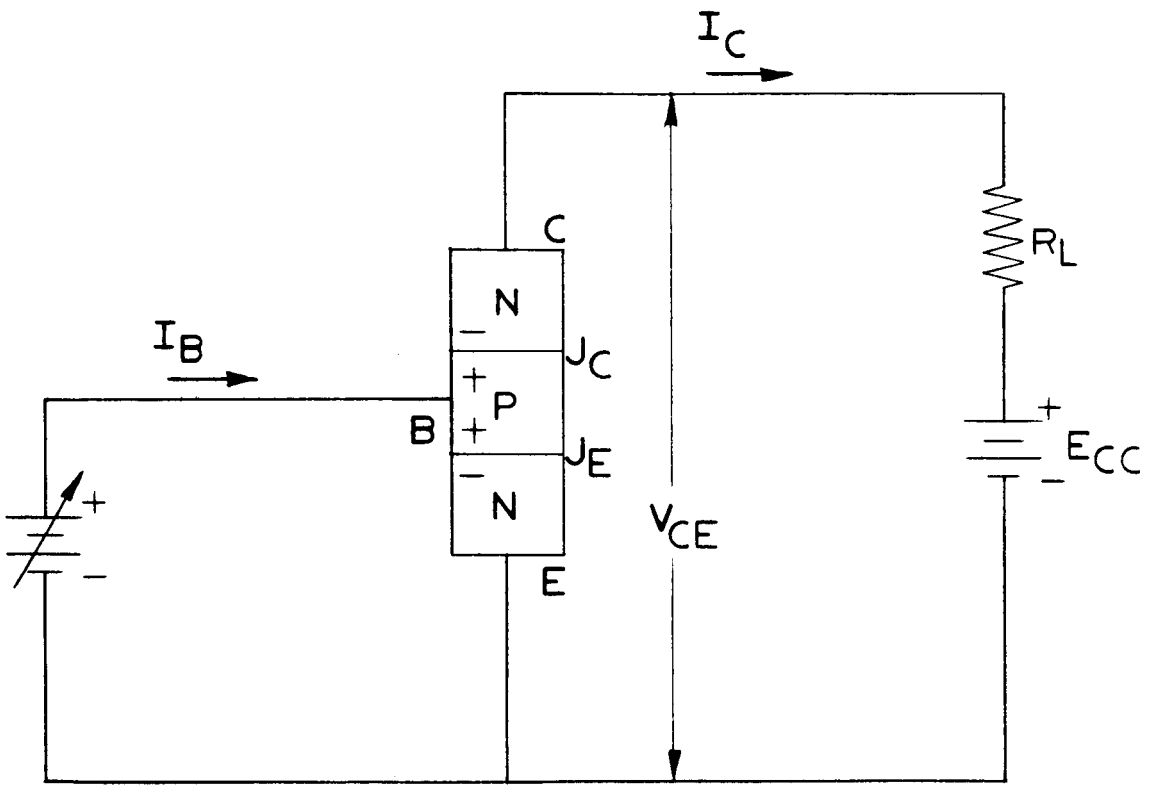


Figure 6

Transistor in Typical Common Emitter Circuit

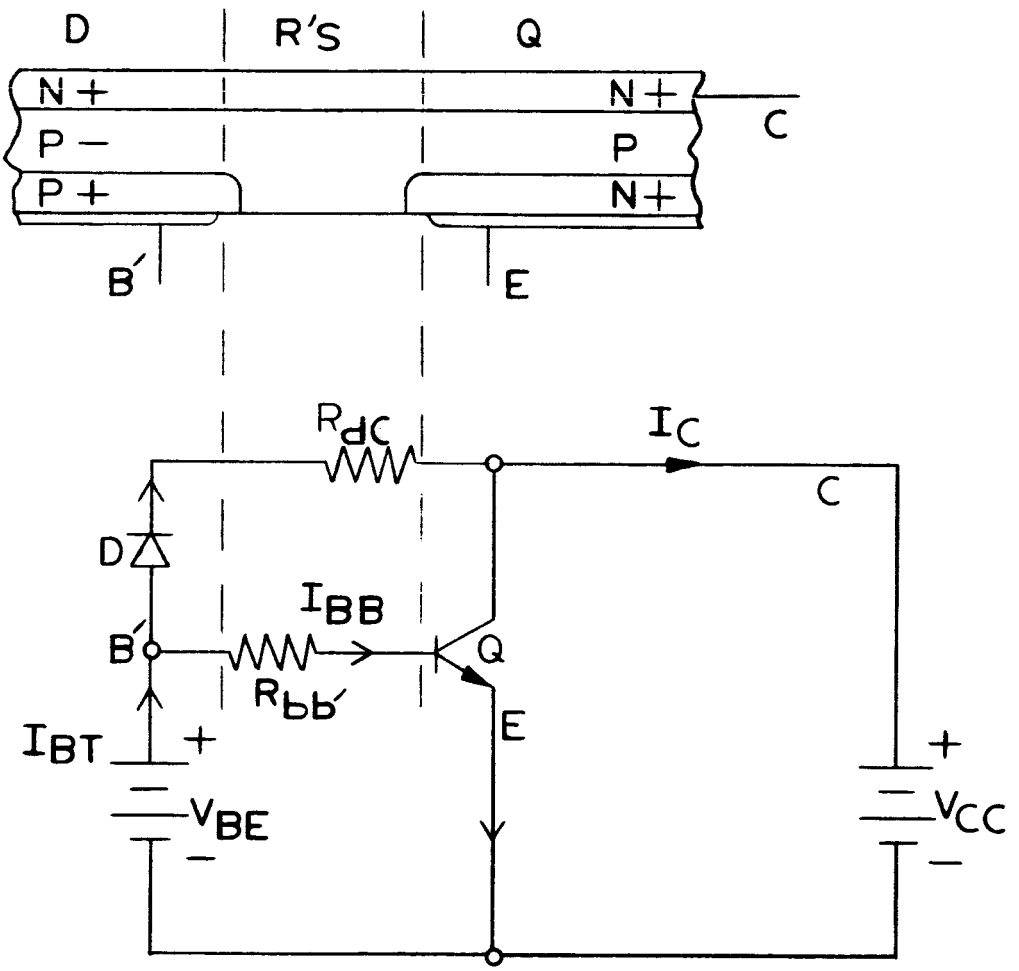


Figure 7

Equivalent Circuit and Collector-Base Contact Overlap

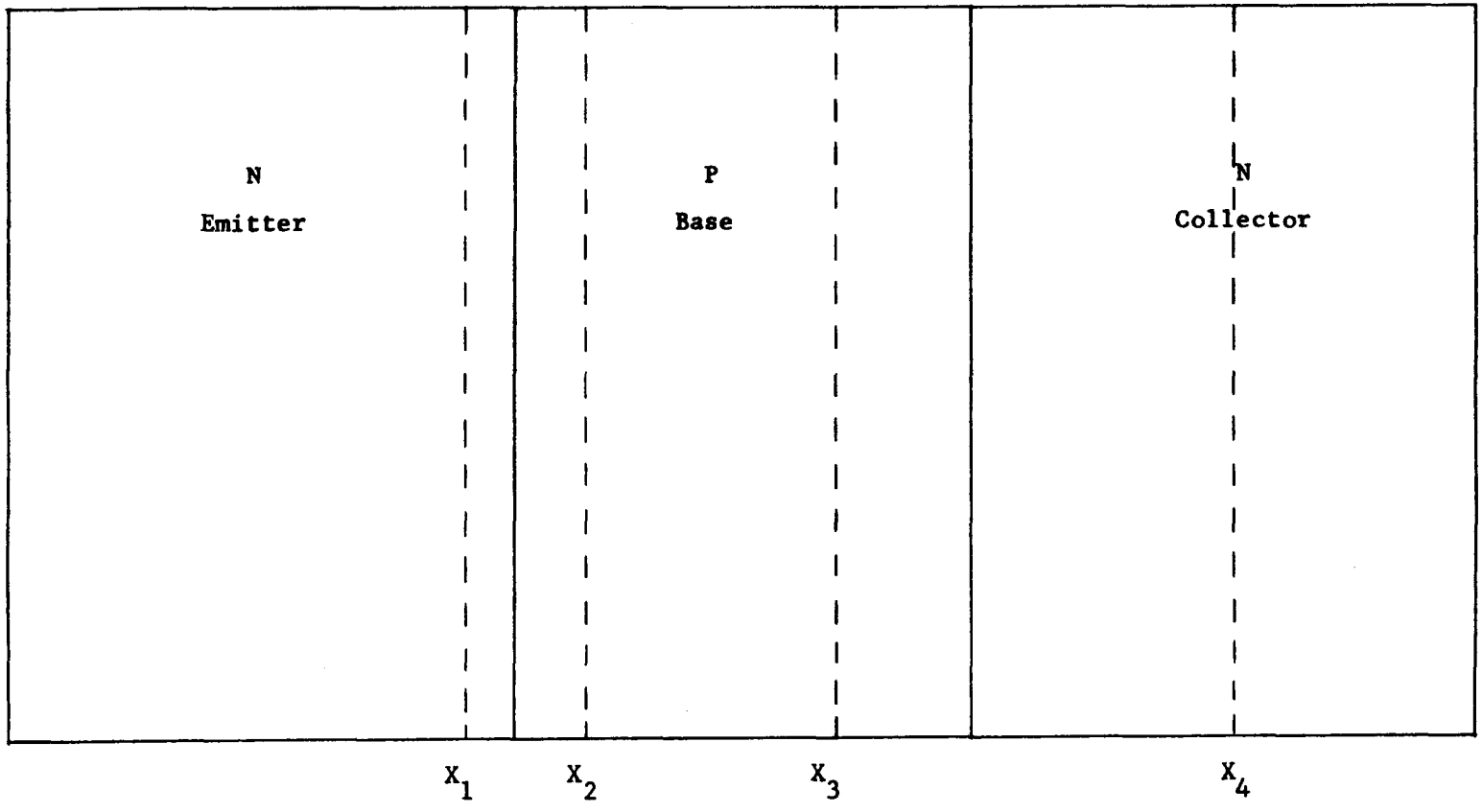


Figure 8

ANALYTICAL MODEL

III. MATERIAL PREPARATION

A. BACKGROUND

The present method for producing silicon epitaxial overgrowth on silicon involves a crystallization from the gaseous phase by the aid of the chemical reaction between silicon tetrachloride and hydrogen at elevated temperatures. Similar such processes have been used for the past 100 years for the production of crystals.

The substrate on which oriented crystallization of a single crystal layer takes place need not consist of a crystal identical to the crystallizing substance. This follows from numerous facts concerning epitaxial overgrowth to which many investigations have been devoted since Frankenheim's[8] time. It is sufficient for the lattice of the substrate to possess the necessary metric and energy compatibility with the crystallizing substance or even for its surface to be compatible in metric and energy respects with at least one principal force of the crystallizing substance. The kinetics and regularities of such growth were thoroughly studied by Dankov[9] who formulated the principle of crystallographic correspondence.

The first stage in crystal growth from the vapor phase must be the formation of a nucleus. This is the smallest number of atoms capable of sustaining further growth, units smaller than this tending to evaporate. This requires molecules to condense into clusters and grow until a critical size has been passed. Clearly, if the pressure of the molecules is very high, i.e., if the vapor is supersaturated then there will be increased tendency for the molecules to condense into clusters and grow into nuclei. The supersaturation required for growth of a nucleus may be very high; indeed, it can be shown supersaturations of about 50% may be necessary. Supersaturation is usually defined as α where

$$\alpha = \frac{\rho}{\rho_o} - 1$$

(8) L. M. Frankenheim, Poggend. Ann., 37, 516, (1936).
(9) P. D. Dankov, "Proc. of the Second Conf. on the Corrosion of Metals," 2, 120, (1943).

ρ = pressure of vapor

ρ_o = equilibrium vapor pressure of the condensed phase at that temperature.

Once formed, the nucleus begins to grow. Atoms from the vapor collide with the nucleus, diffuse over the surface until either they find a suitable site or fly off into the vapor again. Atoms condensing on the surface lose latent heat causing the surface to be at a higher temperature than the bulk of the crystal. Surface temperature 100°C higher than the bulk temperature have been suggested by Wilman[10] as a factor contributing to the mobility of atoms on the surface.

Atoms condensing on the surface will prefer sites with a maximum number of nearest neighbors because at such sites the bonding energy is at a maximum. Occupation of such sites would produce closely packed surfaces over the nucleus. At this point, further condensation becomes difficult. For further growth, sufficient atoms must come together to form an island "nucleus" on the close packed surface. Once formed, the island may grow laterally to the extremities of the surface and then for further growth another nucleus must be formed. This process is similar to the formation of the original nucleus.

The concept of growth by two dimensional nucleation has been considered by several workers and it is possible to estimate the rate of nucleation; i.e., the rate of formation of monolayer islands and also to estimate the degree of supersaturation required to cause detectable growth. The theoretical value of the latter is of the order of 25 to 50%. However, in practice, it has been found that crystals may grow at low supersaturations of about 1%. This anomaly was explained by Frank[11] who proposed the mechanism of crystal growth which follows. He pointed out that if atoms were added onto the steps of a screw dislocation, a close packed surface of the type described in the previous paragraph was never formed but instead a growth spiral resulted. It should be realized that the origin of dislocations and growth spirals is not completely understood. They may be

(10) H. Wilman, Proc. Phys. Soc., London, 1368, 474 (1955).
(11) F. C. Frank, Disc. Faraday Soc., No. 5, 48 (1949).

created in the nucleus by thermal agitation or mechanical deformation or introduced during subsequent development of the nucleus. This suggests that the dislocation density can be reduced if conditions during growth are made as free from fluctuations (thermal and mechanical) as possible.

Since the substrate acts as an initial "nucleus" in epitaxial overgrowth, it might be expected that the perfection of overgrowth would depend upon the crystallographic orientation of the substrate. This has been observed in germanium where it was found that the rate of germanium overgrowth was dependent on the substrate crystal orientation for the most densely packed faces <110>, <111>, and <100>. Owing to the strong bonding forces acting in the planes of these faces, condensing atoms will be oriented in the correct way.

The perfection of overgrowth also depends on the temperature of the substrate. It has been found that silicon overgrowths prepared at a substrate temperature of 1270°C show a high order of perfection while the overgrowths prepared at 1175°C are less perfect. These results suggest that during deposition, the high-surface mobility of silicon atoms attained at 1270°C is essential for good film perfection. The high-surface mobility of silicon atoms enables them to diffuse over the surface and to find correct oriented positions.

A further requirement for the preparation of good epitaxial overgrowth is that the substrate must be free from surface defects. For example, in the case of silicon good epitaxial overgrowth cannot be obtained in the presence of a substrate surface oxide. The latter provides nucleation sites for polycrystalline growth.

In the epitaxial overgrowth of silicon, the deposited silicon is produced by the hydrogen reduction of halosilanes such as silicon tetrachloride, the reduction of which may be represented by the simple equation:

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl.$$

This equation does not predict the observed yield of other chlorosilane compounds or the yield of high molecular weight polymers of the homologous series $(SiCl_2)_xH_2$, such as $Si_{10}Cl_{20}H_2$, found as a condensate on the reaction walls. To account for the reaction products, it is possible to formulate numerous equations which represent possible reaction mechanisms. The standard free energies for a few of these reactions have been calculated (See Table III) and it may be seen that all are thermodynamically possible. An investigation has been carried out to evaluate, by means of gas chromatography, the reaction products of the silicon tetrachloride and hydrogen reaction.

It has been found that the epitaxial overgrowth rate of silicon is effected by the hydrogen to silicon tetrachloride molar ratio and also the hydrogen flow rate. The causes for these effects are not understood completely. It has been suggested that owing to the relatively high activation energy found for the hydrogen-silicon tetrachloride reaction and reduction in growth rate found by increasing the molar ratio above 0.1 that the following mechanism is possible. First there is adsorption of a silicon subchloride, probably the free radical $SiCl_3$, on the substrate surface and this is followed by loss of chlorine by reaction with hydrogen. However, the occurrence of adsorption phenomena at high temperatures seems doubtful and until further work has been carried out, particularly on the identification of reaction products, the kinetics of the reaction of hydrogen with silicon tetrachloride will remain obscure.

B. REQUIREMENTS FOR EPITAXIAL GROWTH

The epitaxial surface requirements for the 100-amp transistors are stringent; no defects are tolerable over the entire large area active region. Small area devices can tolerate several defects since these units can be discarded. However, the presence of one defect in the

100-amp configuration would nullify the unit because of the resultant low voltage or short characteristics. It has been determined that all epitaxial defects originate at the substrate epitaxial layer interface and are dependent on surface cleanliness, substrate perfection and system purity.

1. Substrates

The substrates used for the 100-amp devices are degenerate in that they are heavily doped with impurities. The doping level of the substrate was selected to obtain the designed saturation voltage characteristics. Heavily doped substrates inherently contain sufficient impurities to distort the crystal lattice. Distortions caused by precipitates or inclusions will not permit a sufficiently good lattice match for defect-free epitaxial growth. These distortions can be eliminated by careful selection of the parent crystal growth conditions and the type of dopant. Evaluation of the substrate material is accomplished by examination of the chemically polished surface prior to epitaxial growth. A chemically polished surface was employed for this device to insure a damage-free surface and to permit microscopic examination of the surface before growth was initiated.

2. Substrate Preparation

Preparation of the substrate material before epitaxial growth is a deciding factor in producing defect-free epitaxial layers. Heavy metal impurities, such as aluminum or iron, are retained by the substrate after the slicing and doping operations. These can give rise to foreign nucleation sites during the growth process. Wetting agents or solvents do not effectively remove these heavy metals. However, chemical techniques, such as reactive chloride acids, convert most heavy metals to water soluble metal chlorides and are easily removed by subsequent rinsing in deionized water.

3. Epitaxial System Purity

Epitaxial growth perfection is also dependent on system purity, that is, the environment in which the chemical reduction of the halide takes place.

a. Gas System -- The gases used in the epitaxial process must be of good quality. The hydrogen used for the reduction is passed through a Deoro unit to remove traces of oxygen and then through a dryer to remove water to a purity of less than 1ppm. All gases are filtered through submicron filters to remove foreign particles before they enter the reaction chamber.

The control of the gases, the valving and piping required to mix and dilute, switching and metering are all done in a system that is leak proof. The materials of construction are Teflon and quartz to maintain gas purity prior to the reaction chamber.

b. Reactor -- A horizontal RF heated epitaxial system was used for all the 100-amp device substrates (Figure 9). The susceptor was a pure grade of graphite coated with silicon carbide. The silicon carbide is deposited on the graphite under the same conditions required for epitaxial growth to insure a noncontaminating or defect contributing source.

The reactor tube was of quartz and the susceptor is supported on a quartz sled. Reactor tube and susceptor loading is accomplished in a positive pressure hood to minimize dust or environmental particles from contaminating the surfaces of the slices.

c. Epitaxial Procedure -- The epitaxial procedure for the 100-amp device consists of heating the substrates to 1200°C in a filtered dry hydrogen atmosphere. Pure gaseous HCl is introduced to etch the substrates prior to growth. The reaction of HCl and silicon is the reverse

of the deposition reaction and permits the removal of the last traces of work damage caused by chemical polishing.

$$4HCl + Si \longrightarrow SCl_4 + 2H_2$$

Sufficient silicon is removed to insure a lattice match for the growth operation.

The HCl procedure is followed with a pure hydrogen treatment at 1200°C to clean out the reaction area of any chlorides which could act as nucleation sites. The collector area deposition follows for the designed thickness and the resistivity is controlled to 8-12 ohm-cm N-type. After the collector has been deposited, the system is purged with pure hydrogen at 1200°C to remove the residual traces of the gases from the collector deposition. The P^+ base layer deposition then follows to give a layer of 4-5μ of P, 0.1 ohm-cm. Gaseous dopants such as phosphine and diborane are used to control the resistivity in the epitaxial layers. After the growth of the base layer the system is cooled for removal of the substrates.

C. EVALUATION

1. Resistivity

The resistivity of the grown layers was determined using a three-point and a four-point probe (Figure 10). The collector resistivity was determined by three point readings on a single N^+N^- deposition.

2. Layer Thickness

The thickness of the deposited layers was accomplished by angle lapping and staining techniques. Interference measurements with sodium light were used to determine actual layer thicknesses (Figure 11).

3. Surface Quality

Visual examination, microscopic techniques, and chemical etching of the surface were used for surface evaluation. If any defect was found under visual examination of the active area of the deposited substrate, the

slice was rejected. Units fabricated from slices containing poly inclusions on tetrahedrals always gave low voltages (V_{CB} of 5-10 volts).

The surfaces were also etched in a chromic oxide, hydrofluoric acid, water mixture to determine the number of stacking faults present. Counts of 8-20 per cm^2 were the usual case.

Microscopic examination was used to determine the presence of defects not seen by the visual techniques. However, yields of 90% good electrical units were achieved on those slices that passed through the visual examination.

Table IV compares the electrical characteristics of mesa diodes on one slice with an epitaxial collector and base with mesa diodes etched on a slice with an epitaxial collector and diffused base. Uniformity of deposition is illustrated here as well as the low leakage capabilities of the epitaxial process.

TABLE III

Standard Free Energies for Typical Silicon Reactions

Reaction	Standard Free Energy for Reaction at 1553Å (1270°C)
$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl$	-1.9 Kcal/mol.
$SiCl_4 + Si \rightleftharpoons 2SiCl_2$	-2.2
$SiCl_2 + H_2 \rightleftharpoons Si + 2HCl$	-1.2

TABLE IV

IV Characteristics of Mesas in Diffused and Epitaxial P-N Junctions

Mesa	Diffused Junction After Boron Diffusion	Epitaxial Junction (without Gettering)
1	100V, 80mA	200V, 1mA
2	30V, 80mA	200V, 1mA
3	80V, 80mA	200V, 1mA
4	200V, 15mA	200V, 2mA
5	200V, 5mA	200V, 1mA
6	10V, 90mA	200V, 1mA
7	30V, 90mA	200V, 2mA
8	200V, 15mA	200V, 1mA
9	200V, 15mA	200V, 1mA
10	200V, 8mA	200V, 5mA
11	90V, 80mA	200V, 3mA
12	40V, 30mA	200V, 4mA
13	100V, 90mA	200V, 3mA
14	160V, 50mA	200V, 1mA
15	40V, 50mA	200V, 2mA
16	90V, 80mA	180V, 1mA
17	6V, 80mA	180V, 2mA
18	36V, 90mA	180V, 1mA
19	32V, 90mA	180V, 2mA

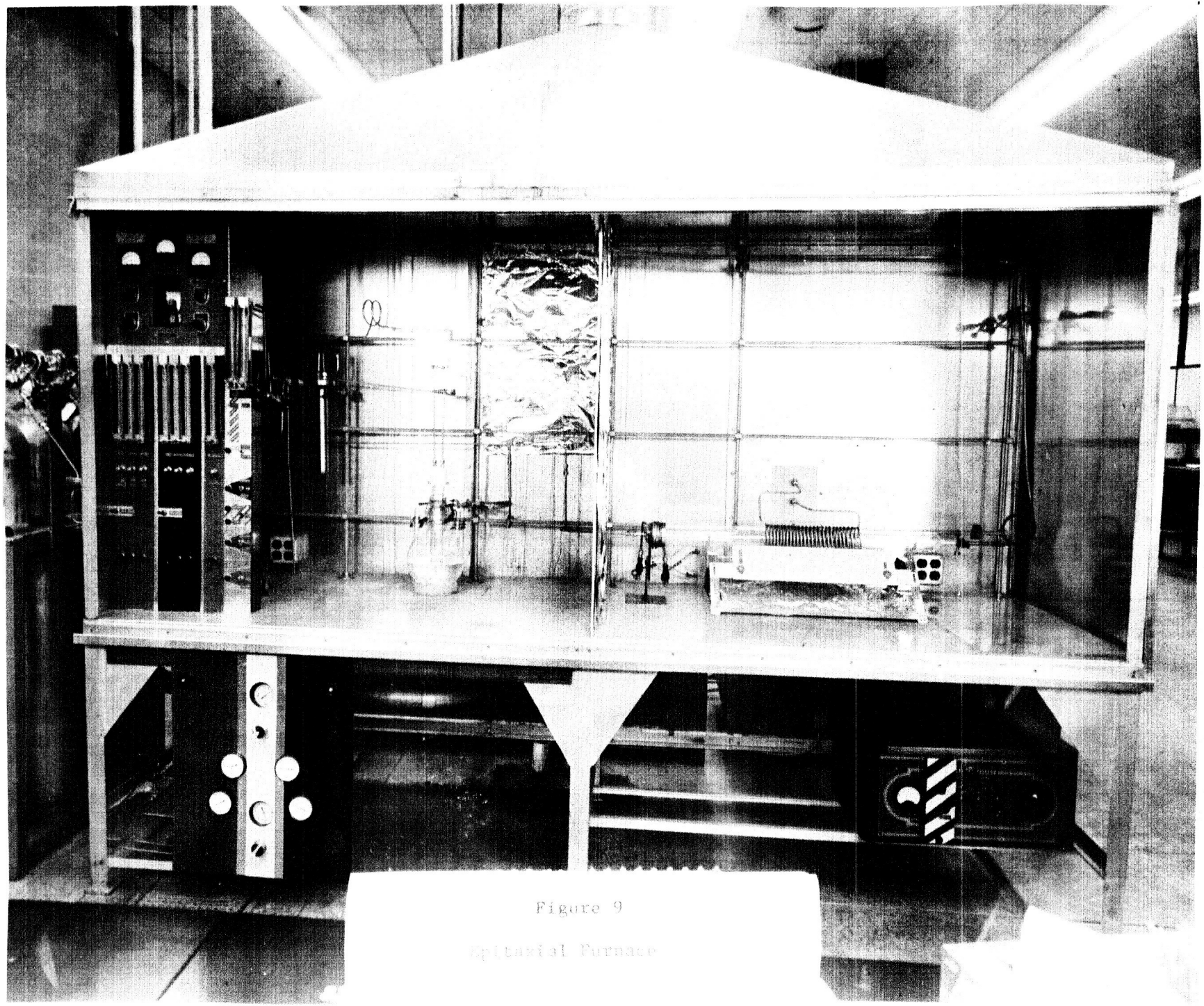


Figure 9

Epitaxial Furnace

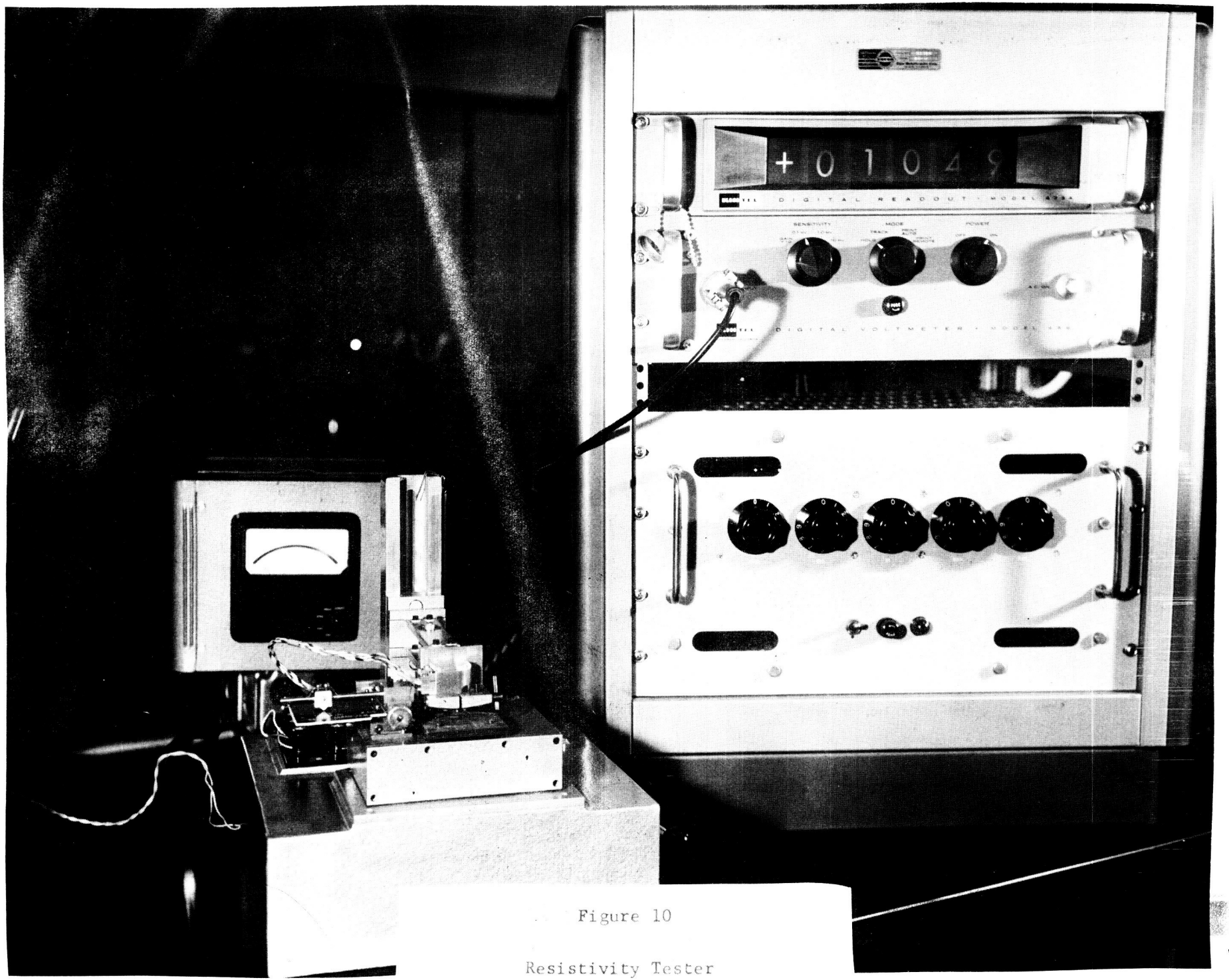


Figure 10

Resistivity Tester

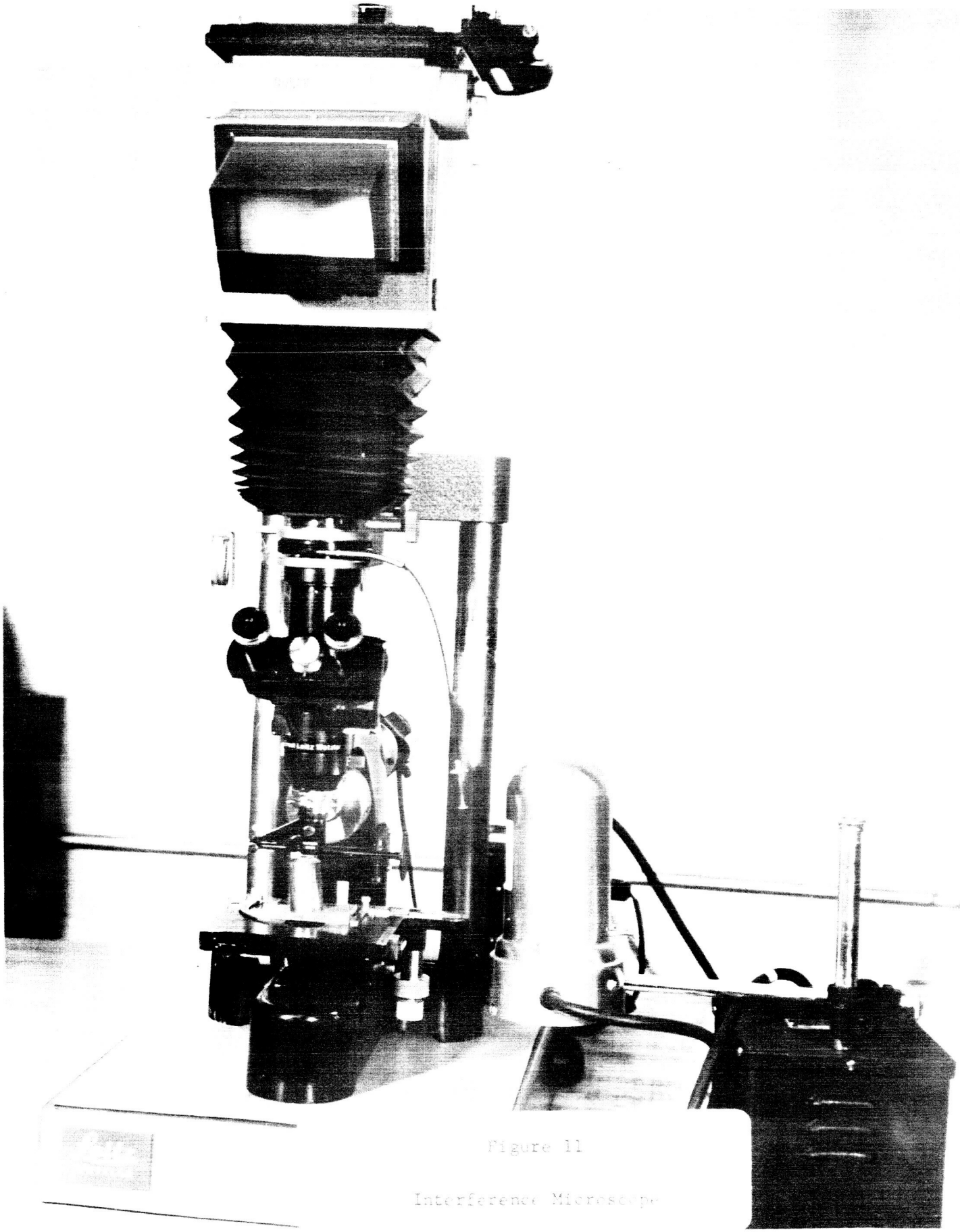


Figure 11

Interference Microscope

IV. DEVICE FABRICATION

Two major processes were used to fabricate the 100A transistor for this contract. In Process A the collector was grown epitaxially and the base and the emitter regions were formed by diffusion. In Process B the collector and the base regions are grown epitaxially and the emitter region is formed by diffusion. The details of these processes are given in this section. These can be more fully appreciated if the flow charts, Figures 12 and 13 are followed as the section is read.

A. PROCESS A - DOUBLE DIFFUSED, SINGLE EPITAXIAL

1. Epitaxial Growth

The details of the epitaxial process are given in the section on material preparation (Section III).

2. Sandblasting

The purpose of the sandblasting was to cut the size of the wafer from 1 inch to .93 inch, which was the size of the moly. The slices were mounted with wax on a copper stud and sandblasted to the size of the moly.

3. Boron Diffusion

The slices were subjected to prediffusion cleaning as described in Table V (which gives in tabular form all the process described below).

A thin layer of boron was deposited on the top of the collector region. The slices were transferred directly to the boron drive-in furnace and were given the required base drive. The control slice was removed, the oxide etched, the sheet resistivity measured by the four-point probe method and the corresponding surface concentration was determined from Irwin's curve.

4. Emitter Masking

The slices were coated with a uniform film of Kodak Metallic Etch Resist (KMER) using a high speed spinner (Figure 14). (The speed of the spinner was 3000 revolutions per minute and the wafer was spun for 45 seconds.) The coated wafer was placed in an oven and baked for 10 minutes at 95°C. One of the slices from each group was used to fabricate control transistors. The wafer was placed on a self leveling alignment fixture. The emitter mask was placed in the fixture and the wafer was brought in contact with it. The mask shown in Figure 15 was used for the control slice and the mask shown in Figure 16 was used for the large area 100A transistor. When the contact and the alignment was completed, an ultraviolet light was used to polymerize the resist which was not protected by the opaque areas of the mask. The unpolymerized resist was then removed by spraying the entire surface with resist developer for 30 seconds. This was then followed by a spray of isopropyl alcohol for 30 seconds. The wafer was blown dry with nitrogen for 30 seconds. The entire pattern was then inspected under a high power microscope (Figure 17). The slices that showed defective patterns had the photoresist stripped off and were recoated with photoresist and the above process was repeated. These wafers were then baked in an oven for 30 minutes at 150°C. The oxide was then etched to expose the area for the emitter diffusion. It was etched for 5 minutes using a solution containing ammonium fluoride and sulfuric acid in the ratio 6:1. It was then rinsed with deionized water and blown dry with nitrogen. The photoresist was then removed from the top of the slices by placing it in hot sulfuric acid (500°C) for 20 minutes. It was then rinsed with deionized water for 5 minutes and placed in hot deionized water (400°C) for 20 minutes. Finally, the slices were blown dry with nitrogen. The slices were then ready for emitter diffusion.

5. Emitter Diffusion

Before emitter diffusion, the slices were given the diffusion cleaning previously explained. The emitter diffusion was done in the furnace shown in Figure 18. The furnace was maintained at a temperature of $1000^{o}C$ over a flat zone of 12 inches.

The wafers to be deposited were removed from the plastic container with tweezers and blown dry with N_2 which passed through a millipore filter. The dried wafer was then placed on the N^+ deposit boat, which was located under a heat lamp (Figure 19). After all the wafers have been dried in this manner with the N_2 jet placed under the lamp, the boat was allowed to remain there for 5 minutes.

Prior to actually placing the wafer-holding boat into the diffusion furnace, the diffusion system had to be purged in the following manner: (1) the source was allowed to flow through the diffusion tube for 2 minutes; (2) the source gas was shut off and the system was allowed to set for 2 minutes; (3) 1 minute was allowed to load the boat which has been under the heat lamp; (4) the boat and wafers were permitted to remain in the flat zone for 2 minutes. This was done to allow boat and wafers to reach the flat zone temperature before starting the diffusion cycle; (5) the carrier gas was allowed to flow through the BBr_3 source and through the diffusion tube for 60 minutes; (6) at the conclusion of the run, the source was shut off and the wafer permitted to sit in the flat zone for an additional 2 minutes; (7) the boat was withdrawn and the wafer allowed to cool to room temperature.

Upon completion of the N^+ deposition cycle, it is essential that the surface concentration of the deposited layer be determined. This was found from the sheet resistivity (ρs) and depth (X_j) of the layer.

The oxide was etched by immersing the wafers in concentrated (48%) hydrofluoric acid for 2 minutes. After the HF etch, the wafers were rinsed in running deionized H_2O for 3 minutes and dried under a heat lamp.

The dried wafer was then placed in the four-point probe and the sheet resistivity read. The junction depth was done by sectioning a portion of a deposited wafer on a 3^{o} angle block. Such a portion was first mounted on the beveled part of the block with wax. After allowing the wax to harden, the samples were polished on a polishing wheel. The liquid and solid polishing materials were then removed by gently swabbing the sample with a warm, mild soap solution. This was followed with a thorough rinse under running deionized H_2O (at least 1 minute). The sample was then blown dry with filtered nitrogen. It was now ready to be stained with the proper acid to delineate the junction. A photographic record of the interference fringes was then obtained (Figure 20) and thus junction depth was directly measured.

The surface concentration of the deposited layer was determined from Irwin's curves.

6. Emitter-Base Contact Masking

The contact areas on the slices were exposed using the emitter base contact mask. The mask used for the large area 100A transistor is shown in Figure 21, and that used for the small area 10A transistor is shown in Figure 22. The photomasking and the etching were done as described above. The collector side of the slices were sandblasted. The slices were then mounted on glass plates with the collector side exposed and it was then sandblasted and cleaned to remove the possible deposition of P^{+} layer on the collector side. The slices were now ready to mount on moly.

7. Hard Soldering - Mounting on Moly

Four factors are necessary for successful "hard soldering;" these are: (1) removal of surface films; (2) attainment of a proper cycle of time, temperature and atmosphere; (3) planar control (flatness); and (4) surface finish (roughness). Each of these were achieved. The first by proper extensive cleaning methods, the second by a high vacuum cycle, the third by a lapping operation and the final factor by an etching processing. These are described in detail in Table V .

8. Metalizing

The purpose of metal contacting is essentially to produce a low resistance electrical path between the active junction area and the three external leads of the packaged transistor. Therefore, the requirements for transistor metalizing are the same as those for any other passive electrical connector. These requirements are: (1) ohmic contact between the materials that it connects; (2) lowest possible voltage drops within the body of the contacting metal; (3) electrical isolation of metals at different potentials. Aluminum was chosen as the metalizing material because it appeared to possess the greatest potential for fulfilling the requirements of a good masking procedure combined with etching of the metal.

A low resistance ohmic connection can be made between aluminum and silicon through the eutectic alloy formed at 570°C. Alluminum can be applied to a silicon surface by vacuum evaporation.

Prior to evaporation, the wafers are surface cleaned. Two tungsten coils are placed in the evaporator and each is loaded with sufficient aluminum to evaporate 40,000Å. The cleaned wafers are placed two-inches away from the two coils. The system is then evacuated to the final evaporation pressure of 10^{-6} torr. Each coil is evaporated separately at 5-minute intervals. The photograph of the aluminum evaporator is shown in

Figure 23. The final thickness of aluminum should be 40,000 to 60,000Å, as determined by the design considerations. The wafers are immediately transferred to the photoresist area.

9. Inverse Masking

The inverse emitter base contact mask was used to define the aluminum pattern. Figure 24 shows the mask for the 100A module and Figure 25 the mask for the 10A module.

10. Alloying

The electrical contact made between the evaporated aluminum film and the silicon surface after evaporation is nonohmic. A heat treatment is necessary to lower this contact resistance; however, it is not necessary to heat the wafers to the aluminum-silicon eutectic temperature to achieve the ohmic contact, since surface alloying occurs at temperatures ranging from 500 to 570°C.

Prior to heat treating, the wafers are cleaned to remove surface contaminants. The wafers are placed in a clean quartz boat and inserted into the hot zone of a nitrogen flushed open-tube furnace. The wafers are then cooled in dry nitrogen.

11. Mesa Etching

The collector-base junction was exposed by mesa etching. The mesa mask used for the 10-amp transistor is shown in Figure 26, and that used for the 100-amp transistor is shown in Figure 27. The photomasking, oxide etching and the removal of photoresist were done exactly as described before.

12. Junction Coating

The exposed junction of the 100-amp was carefully coated with glycerin and baked in an oven for 16 hours at 800°C. After 16 hours, the transistors were removed from the oven, were allowed to cool and were tested for electrical characteristics. Those transistors that showed good electrical characteristics were used for encapsulation.

B. PROCESS B - DOUBLE EPITAXIAL, SINGLE DIFFUSED

After several transistor lots were fabricated and evaluated it was determined that although the gain was adequate the devices exhibited poor voltage characteristics. Several approaches were taken to isolate the problem.

1. The large units were etched into small mesas and the voltages of the mesas measured. The voltages for both the large and small units are given in Table VI. It is seen that the voltages of some of the small mesas are considerably better than that of the large unit. This seems to indicate that low voltage of the large area transistor was mainly due to the non-uniform quality of the epitaxial growth over a large area.

2. The quality of the diffusion process was then examined. The base diffusion was done on 20 ohm-cm non-epitaxial slices and BV_{CBO} of each slice was measured. The emitter diffusion was done on the top of the base diffused layer. Both diffusions were done without any oxide masking. The results show that most of the slices have $BV_{CEO} >$ 150 volts at 500 ma, which indicates that the diffusion process is capable of producing high voltages. But the leakage seemed to be quite high. Effort was also expended to see whether voltages could be improved by locating and removing defective areas of the device. The results show that voltage is improved when the defect is removed.

To eliminate the problem of low voltage and high leakage of large area devices, an investigation was started with the collaboration of the Westinghouse Research group. This investigation consisted in: (1) locating the structural imperfections introduced during the epitaxial growth and diffusion process, and (2) introducing techniques to eliminate these imperfections.

As a part of these investigations, an alternate process was initiated. The collector and the base regions were grown epitaxially and the emitter region was formed by diffusion. The voltages (V_{CB}) of the large area slices were measured. After the base growth, one of these slices was etched into small mesas and voltage was again measured. The emitter diffusion was done over the whole base region and the voltage (V_{CE}) was again measured. The results indicate that the breakdown characteristics of the epitaxially grown junction are very uniform and the leakage is very small.

As a result of these investigations, it was decided that double-epitaxial single diffused design should be used to process the transistor for this contract.

Process B differs from Process A by the insertion of two steps between the growth of the epitaxial collector and the emitter masking. This addition was accompanied by the elimination of the boron diffusion step. The additions are:

1. Epitaxial Base Growth

This is essentially similar to the previous step, epitaxial collector growth.

2. Oxidation

After growing the collector and base regions epitaxially, the slices were directly transferred to the oxidation furnace. The oxide layer was deposited at a temperature of 1000°C for 120 minutes to give an oxide thickness of 4000Å. The slices were then mounted onto a copper stud with wax and sandblasted as described earlier.

TABLE V

100-AMP PROCESS DETAILS

PRE-DIFFUSION CLEAN

1. Hot sulfuric acid -- 15 minutes
   Temperature -- 250
2. Rinse deionized water -- 5 minutes
3. Hot nitric acid -- 15 minutes
   Temperature -- 200
4. Rinse deionized water -- 10 minutes
5. Hot triple-distilled water -- 5 minutes
   Temperature -- 350
6. Second hot triple-distilled water -- 5 minutes
   Temperature -- 350
7. Store triple-distilled water

COATING

1. Coat with 2:1 KMER
2. Spin for 45 seconds, 3000rpm
3. Bake 10 minutes in 95° oven

EMITTER MASK

1. Mask No. 142-1B
2. Expose for 20 seconds
3. Spray with developer for 30 seconds
4. Spray with propanol alcohol for 30 seconds
5. Spray with nitrogen air for 30 seconds
6. Bake 30 minutes in 150° oven

ETCH OXIDE

1. 6:1 oxide etch
   a. 6 - ammonium fluoride
   b. 1 - HF
2. Etch for 5-6 minutes until oxide is removed, rinse deionized water, air dry nitrogen
3. Remove photoresist
   a. Hot sulfuric acid - for 20 minutes; temperature 500
   b. Place second sulfuric acid - for 15-20 minutes
   c. Rinse deionized water - 5 minutes
   d. Place hot deionized water - 20 minutes; temperature 400
   e. Place second deionized water - 20 minutes; temperature 400
   f. Air dry nitrogen

(continued on following page)

TABLE V (continued)

EMITTER BASE CONTACT MASK

1. Same as for emitter mask
2. Oxide etch for 3-4 minutes
3. Remove photoresist as before

CLEANING OF MATERIALS FOR HARD SOLDERING

1. Ohmic Solder
   a. Boil in trichloroethylene for at least 2 minutes; do not allow the trichloroethylene to boil dry.
   b. Rinse in alcohol thoroughly.
   c. Rinse again in alcohol.
   d. Dry parts using clean paper towels.
   e. Etch parts for 10 minutes, agitating container for the whole 10 minutes. Etchant: 5 parts nitric acid, 1 part HF.
   f. Flush etchant and parts with alcohol after 10 minutes of etching; agitate vigorously.
   g. Rinse in deionized water several times.
   h. Place parts in clean beaker of water and ultrasonic rinse for at least one minute.
   i. Rinse in deionized water.
   j. Rinse in alcohol several times.
   k. Dry parts using clean paper towels.
   l. Place parts in clean petri dish for storage until use.
2. Moly
   a. Boil in trichloroethylene for at least 2 minutes; do not allow the trichloroethylene to boil dry.
   b. Repeat #1 if parts are excessively greasy.
   c. Rinse in alcohol thoroughly.
   d. Repeat #3.
   e. Etch parts; have three containers placed in bottom of sink, in container #1 put etchant consisting of: 5 parts water (deionized), 5 parts nitric acid, 1 part sulfuric acid. In the second container put concentrated hydrochloric acid (HCl) and in the third container put deionized water. Etch as follows: container #1 - 5 seconds; container #2 - 10 seconds; container #3 - rinse thoroughly. Part container should be moved quickly from one container to the next without delay between etches.
   f. Rinse parts in running deionized water.
   g. Place parts in a clean beaker of water and ultrasonic rinse for at least one minute.
   h. Rinse thoroughly in deionized water.
   i. Rinse in alcohol.
   j. Repeat rinse in alcohol.
   k. Dry parts using clean paper towels.
   l. Place parts in clean petri dish for storage until use.

(continued on following page)

TABLE V (continued)

3. Silicon Devices
   a. Boil parts in trichloroethylene for at least 2 minutes; do not allow the trichloroethylene to boil dry.
   b. Repeat #1 if parts are excessively greasy.
   c. Rinse thoroughly in alcohol.
   d. Dry parts using clean filter paper and clean paper towels.
   e. Etch for 5 minutes in concentrated HF.
   f. Rinse in deionized water several times.
   g. Rinse in alcohol thoroughly.
   h. Dry parts using clean filter paper and clean paper towels.
   i. Place Parts in clean petri dish for storage until use.

   (NOTE: Place parts in glass slice holder for step 'a'.)

INVERSE EMITTER BASE CONTACT MASK

1. After aluminum evaporate
2. Coat KMER as before
3. Bake 10 minutes
4. Same exposure as before and same developing time as before
5. Bake 15 minutes 150° oven

ALUMINUM ETCH

1. Aluminum etch -- 400 phosphoric, 40 nitric, 100 H_2O
2. Etch until aluminum is removed from eitter-base contact area
3. Rinse in deionized water
4. Air dry nitrogen

ALLOY

1. One minute nitrogen furnace

SANDBLAST BACKS AND ETCH

1. Etch for 2 minutes in silicon etch
2. Silicon etch -- 15 nitric, 5 acetic, 1 HF

SANDBLAST FOR MESA AND SPIN ETCH

1. Spin etch for 45 seconds, 5:1:1 -- 5 nitric, 1 phosphoric, 1 HF
2. Rinse for 3 minutes in deionized water; spin dry for 2 minutes

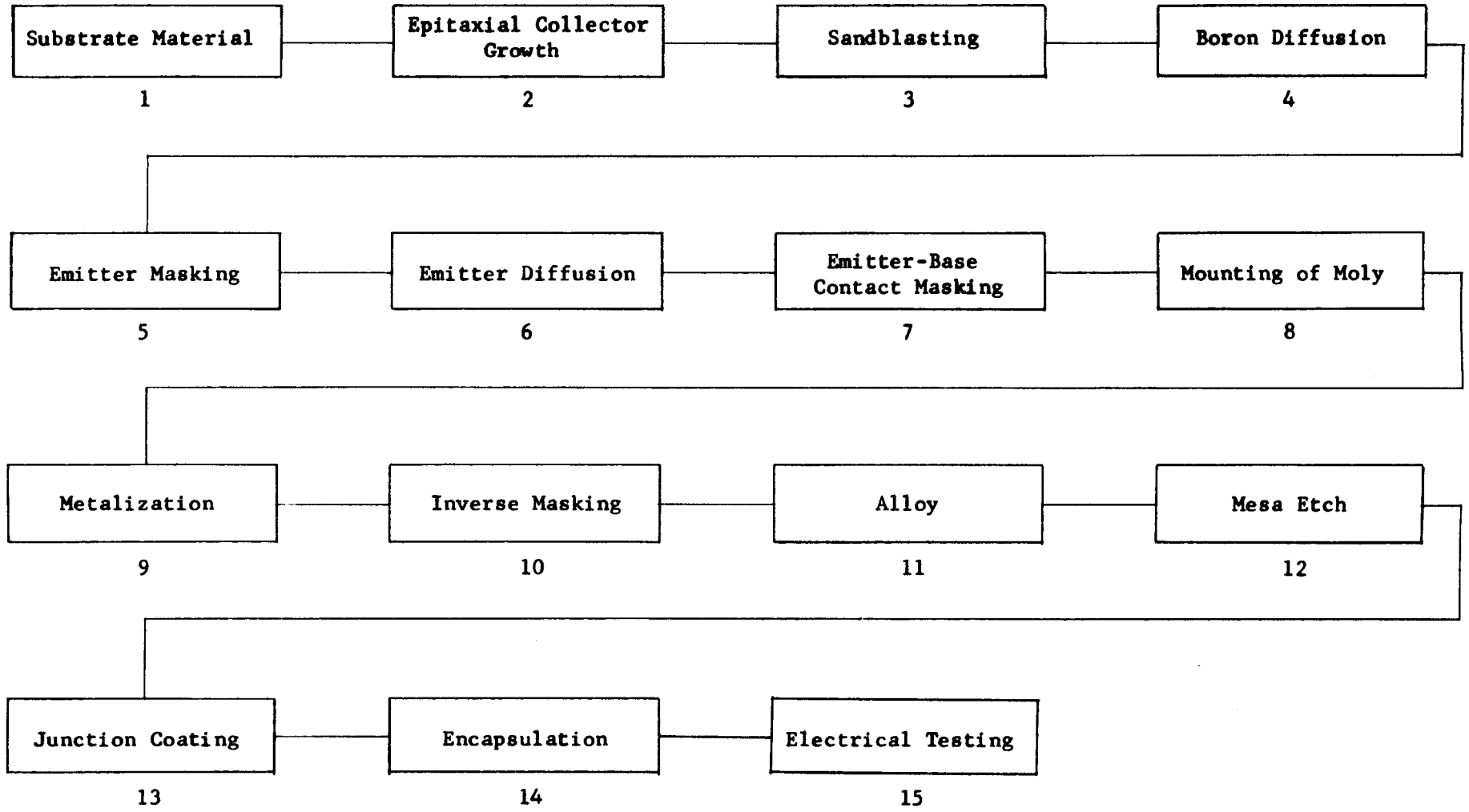
MOUNTED ON MOLY

1. Sandblast and spin etch same as before

TABLE VI

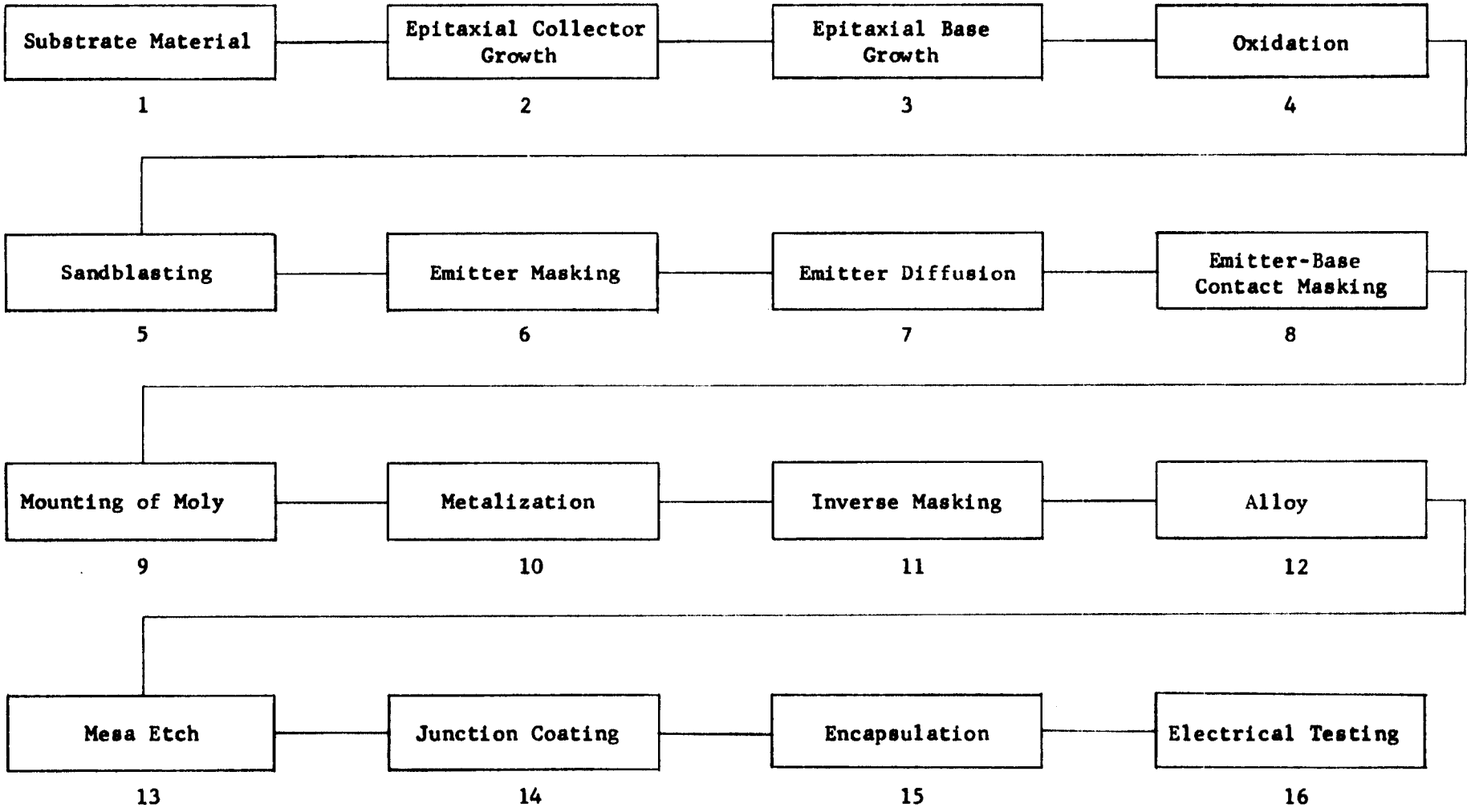
Results of the Small Mesas Etched out of Large Mesas

Mesa No.	P-28(volts)			P-29(volts)			P-30(volts)			P-31(volts)		
	BV_{CBO} 5ma	BV_{EBO} 1ma	BV_{CEO} 10ma	BV_{CBO} 5ma	BV_{EBO} 1ma	BV_{CEO} 10ma	BV_{CBO} 5ma	BV_{EBO} 1ma	BV_{CEO} 10ma	BV_{CBO} 5ma	BV_{EBO} 1ma	BV_{CEO} 10ma
1	150	8	100	10	.5	3.5	33	7	28	19	1.8	15
2	80	8	35	4	.7	6.5	14	4	4	30	7	27
3	45	4	50	14	1	6	47	8.5	43	80	7.5	18
4	120	8.5	100	8	.2	1	23	8.5	23	broken unit		
5	130	9	18	12	2	2.5	23	8.5	7.5	43	7.5	11
6	35	8.5	9	11	2	2.5	30	8.5	10.5	48	8.5	14.5
7	80	1	55	12	.5	5.5	15	8.7	11	20	1.8	25
8	100	1.5	105	9	2	.1	18	8.7	13	broken unit		
9	150	5.5	60	12	2	7	11	2.8	11	38	7.5	15
10(base only)	190	---	---	170	---	---	130	---	---	40	---	---
11	130	7	35	14	8	1.5	48	1.5	28	43	8.5	2.5
12	70	1	45	12	2	2	10.5	1.5	2.5	broken unit		
13	130	8	25	12	4	5.5	28	1.8	22	broken unit		
14	130	8.5	23	12	8.5	9	32	9	12	60	7	19
15	180	8.5	80	12	2	8.5	46	9	17	28	8.5	11
16	45	1	85	15	8.5	6	broken unit			43	1	37
17	150	1	110	14	8	5.5	6	4	32	30	8.5	22
18	70	7	20	13	3	1	broken unit			28	8.5	8.5
19	100	8	90	17	5	12	broken unit			broken unit		
	100ma	100ma	100ma	100ma	100ma	100ma	100ma	100ma	100ma	100ma	100ma	100ma
Large unit	17	7	7	2	1	1	12	8	4	25	5	16



PROCESS A - FLOW CHART

Figure 12



PROCESS B - FLOW CHART

Figure 13

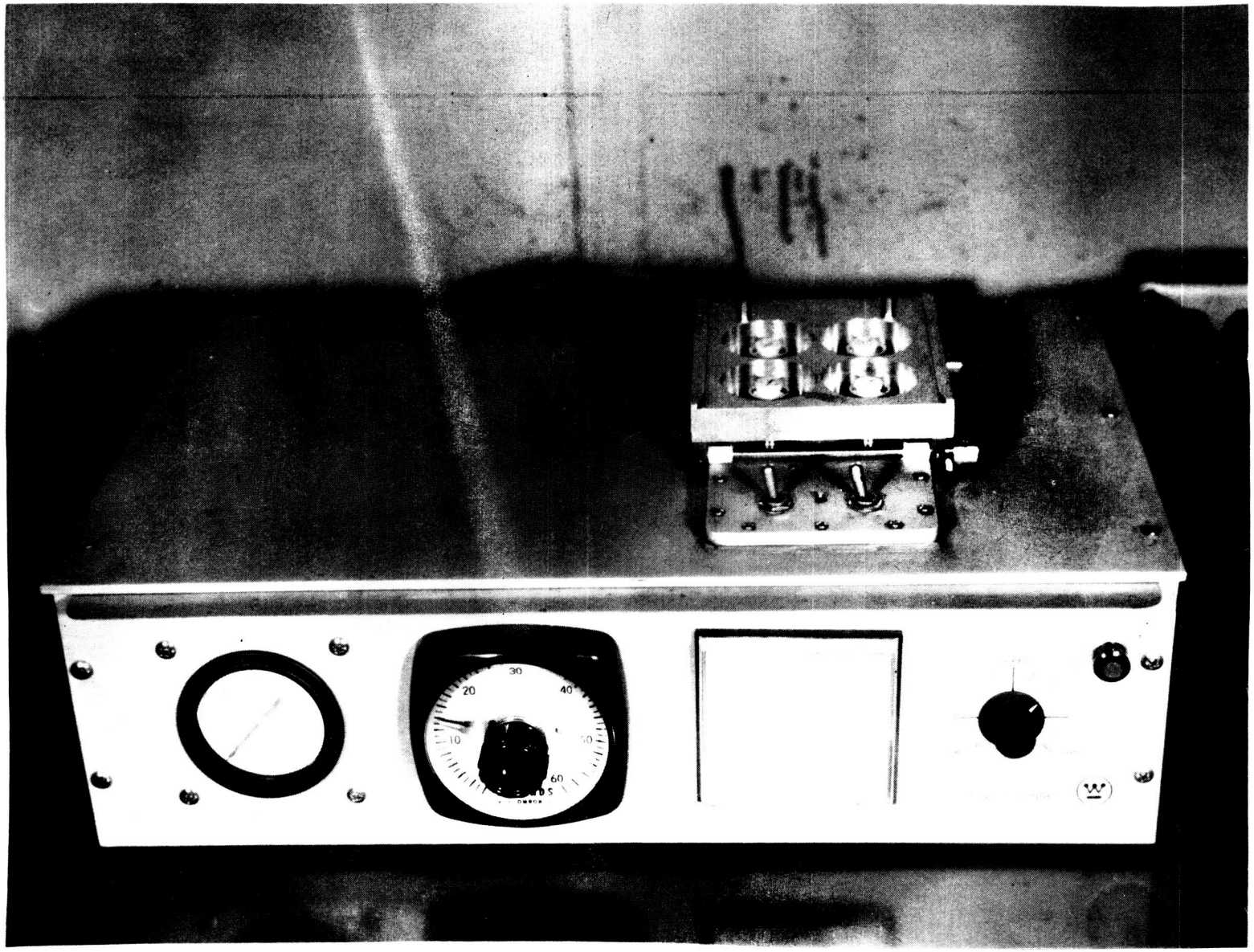


Figure 14

High Speed Multi-Head Spinner

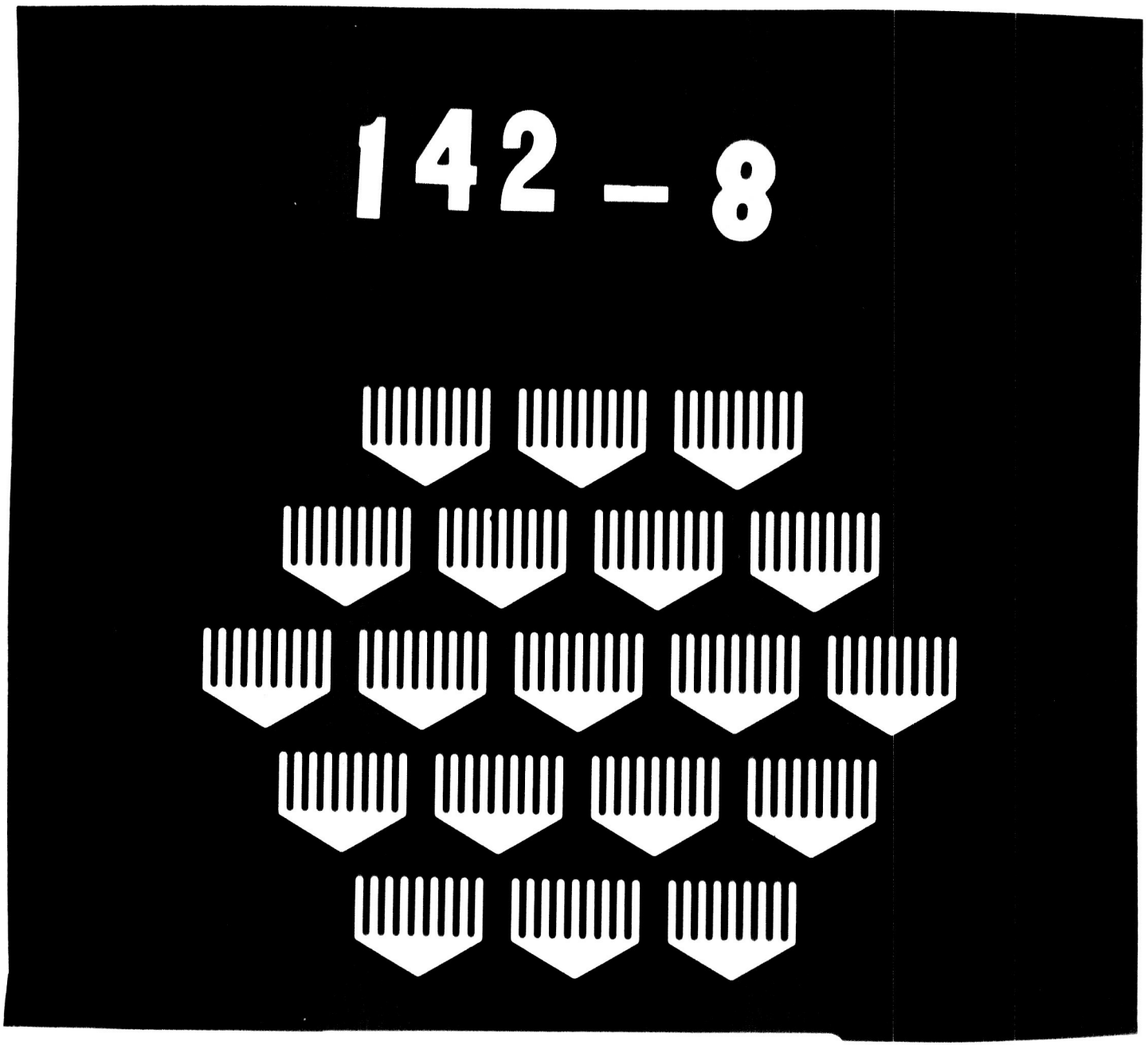


Figure 15

Emitter Mask for Control Slice

142-1B

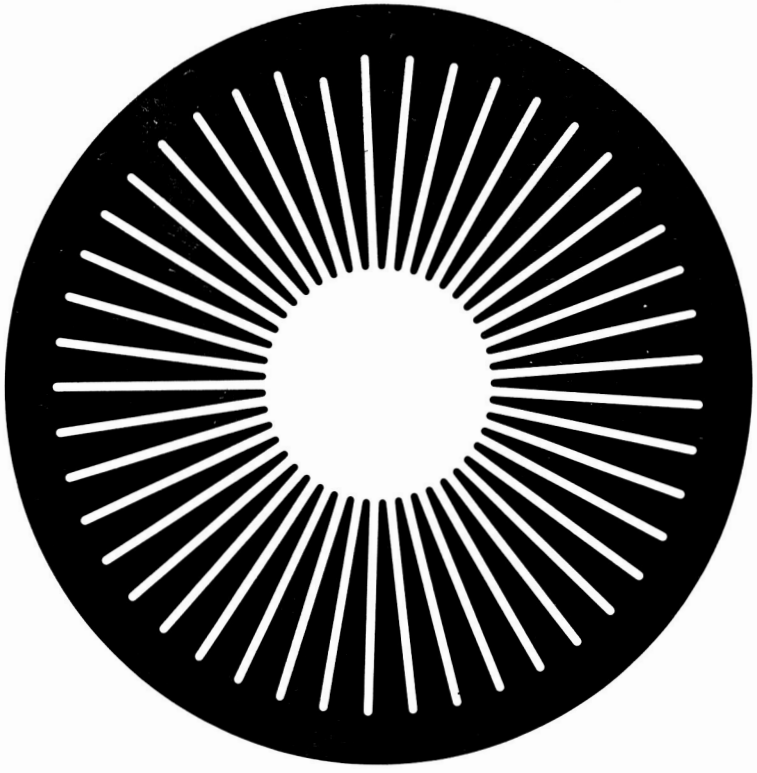


Figure 16

Emitter Mask for Large Area
100A Transistor

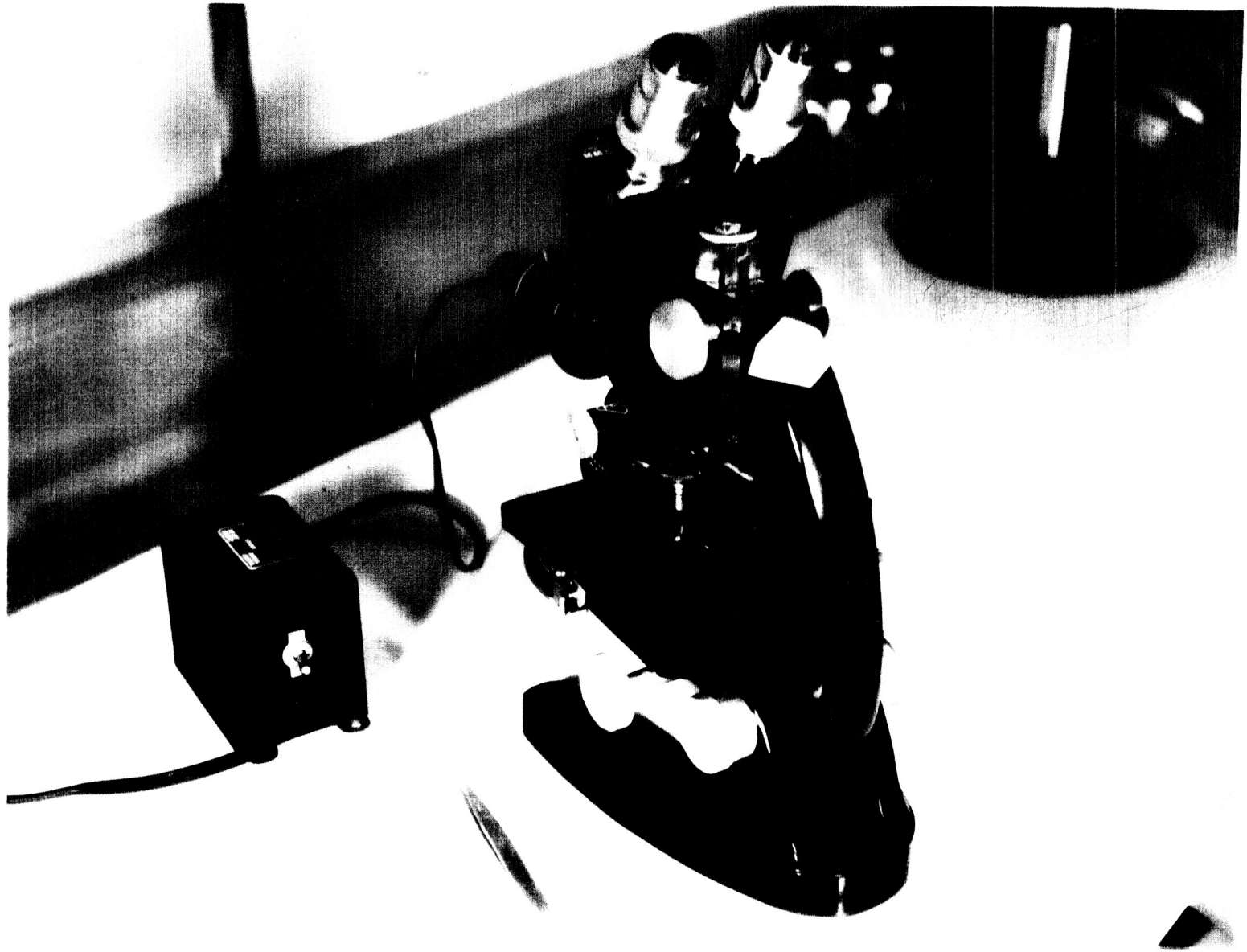


Figure 17

Inspection Microscope

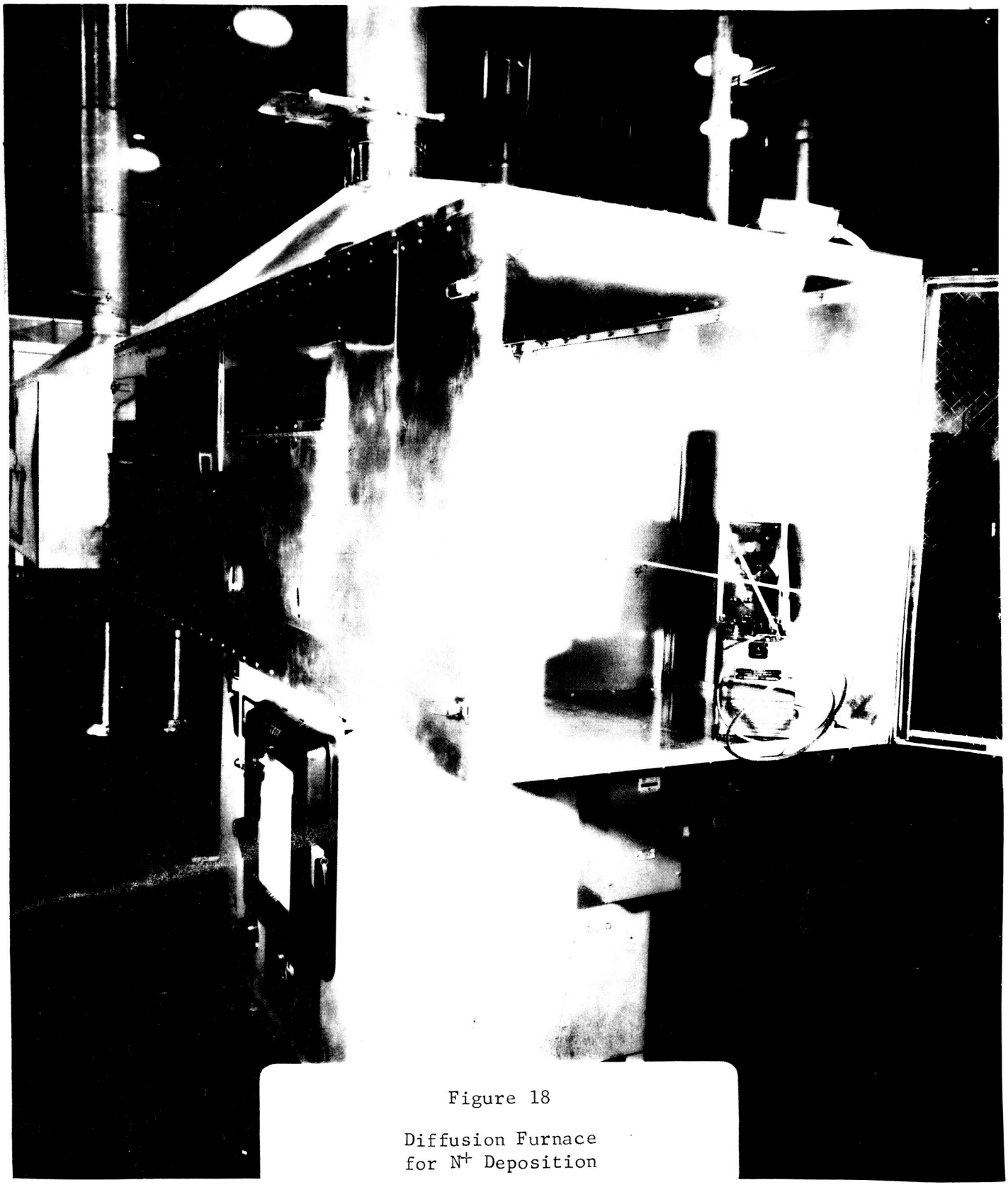


Figure 18

Diffusion Furnace
for N^+ Deposition

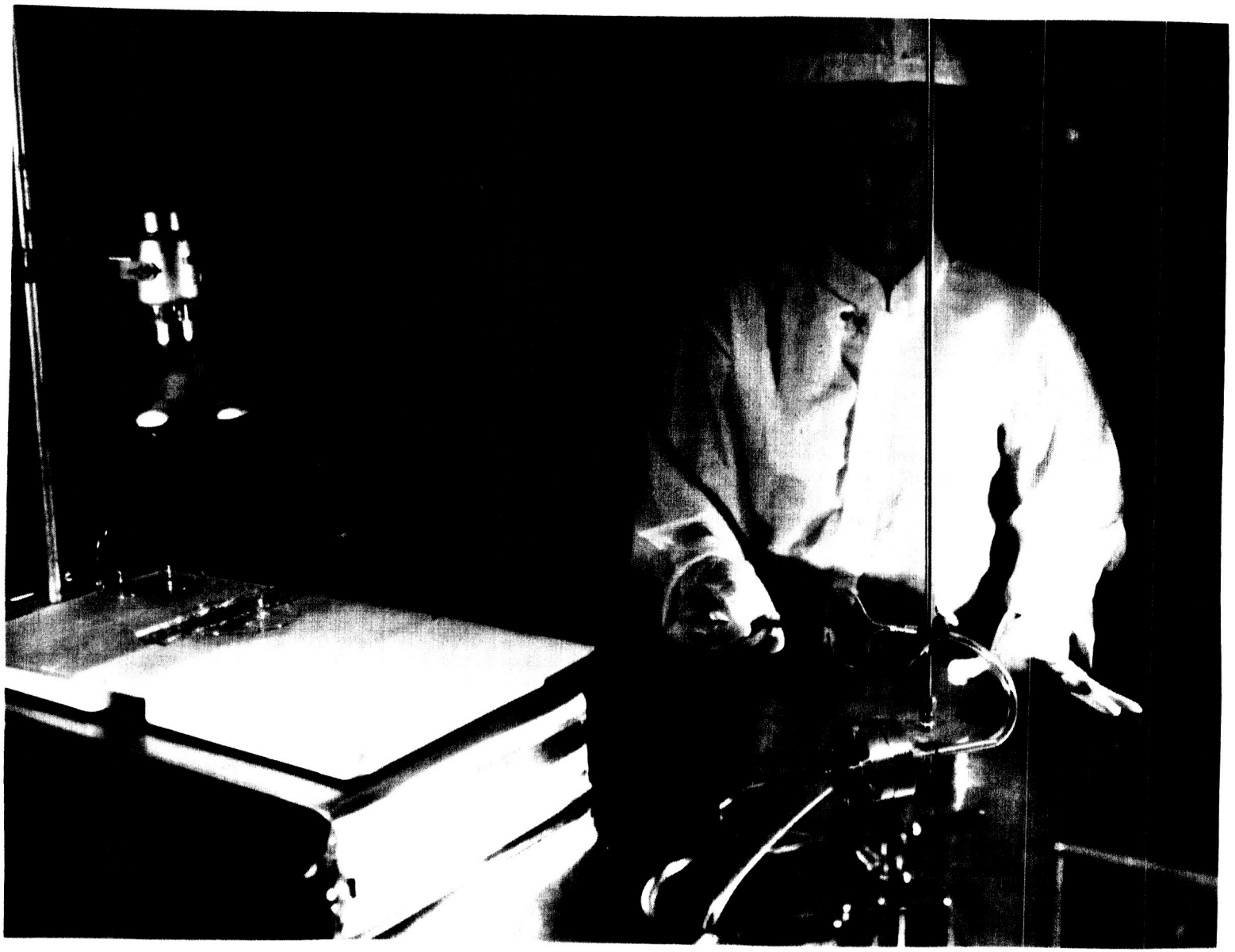


Figure 19

Heat Lamp

Figure 20

Photograph of Interference Fringes

142-3B

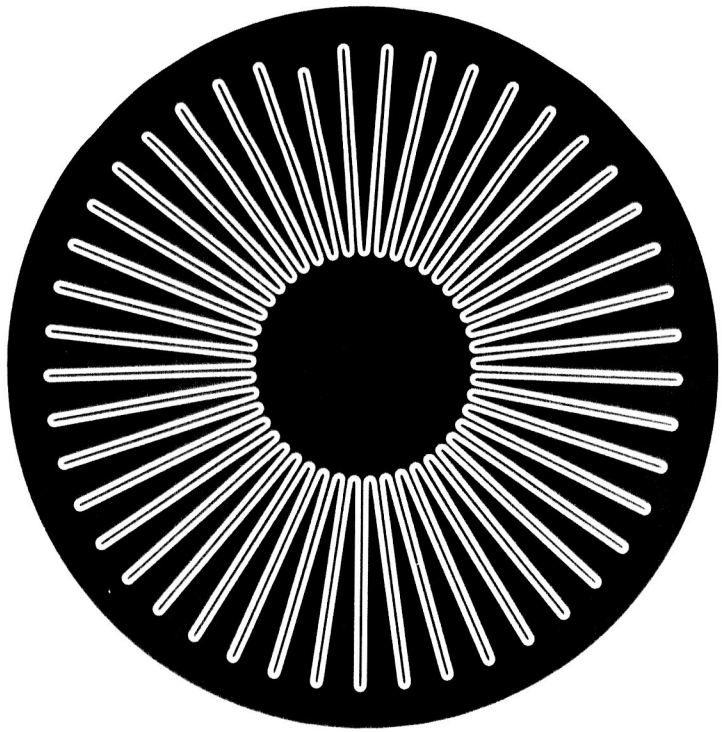


Figure 21

Emitter-Base Contact Mask
Large Area 100A Transistor

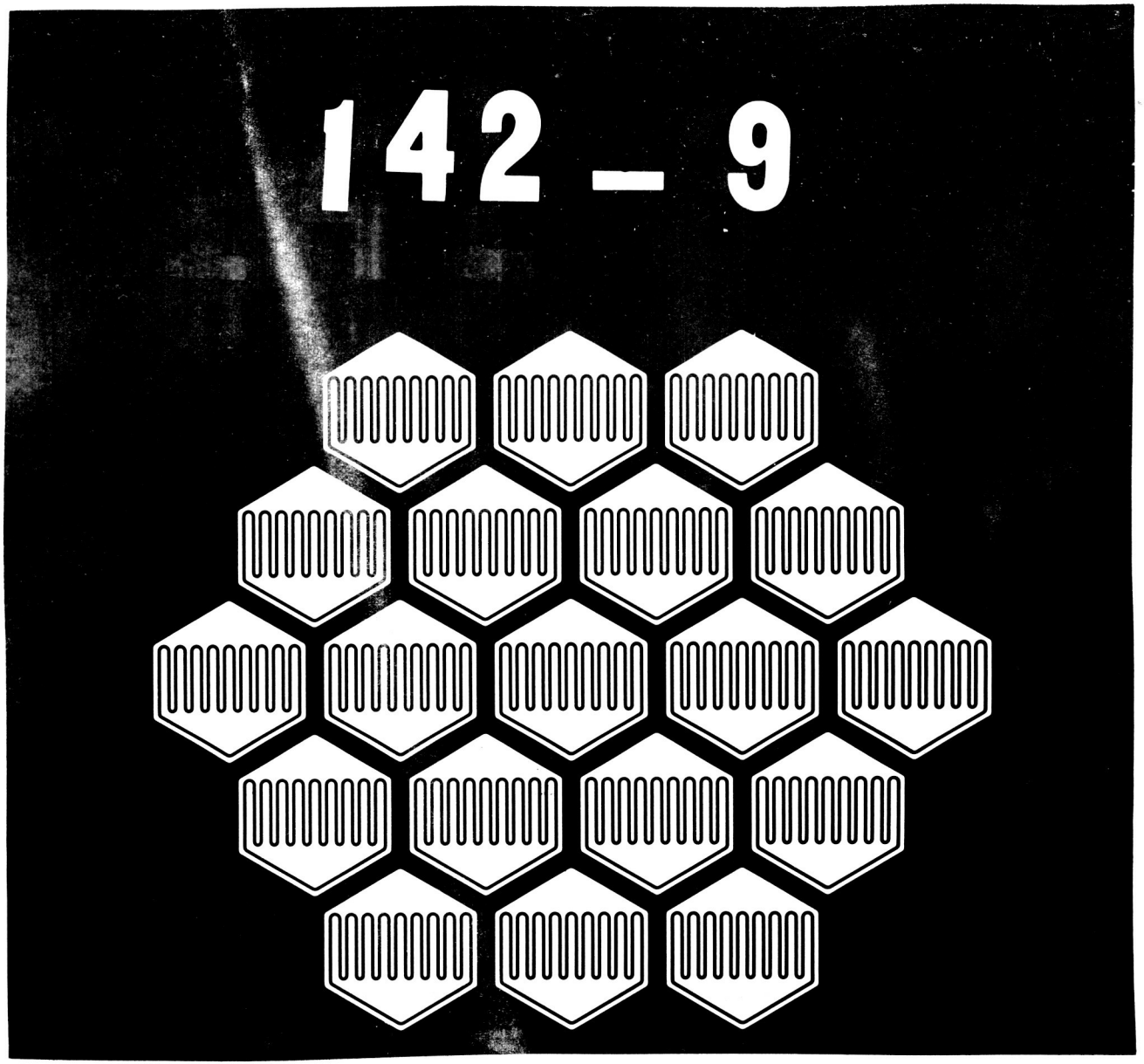


Figure 22

Emitter-Base Contact Mask
Small Area 10A Transistor

Figure 23

Aluminum Evaporator

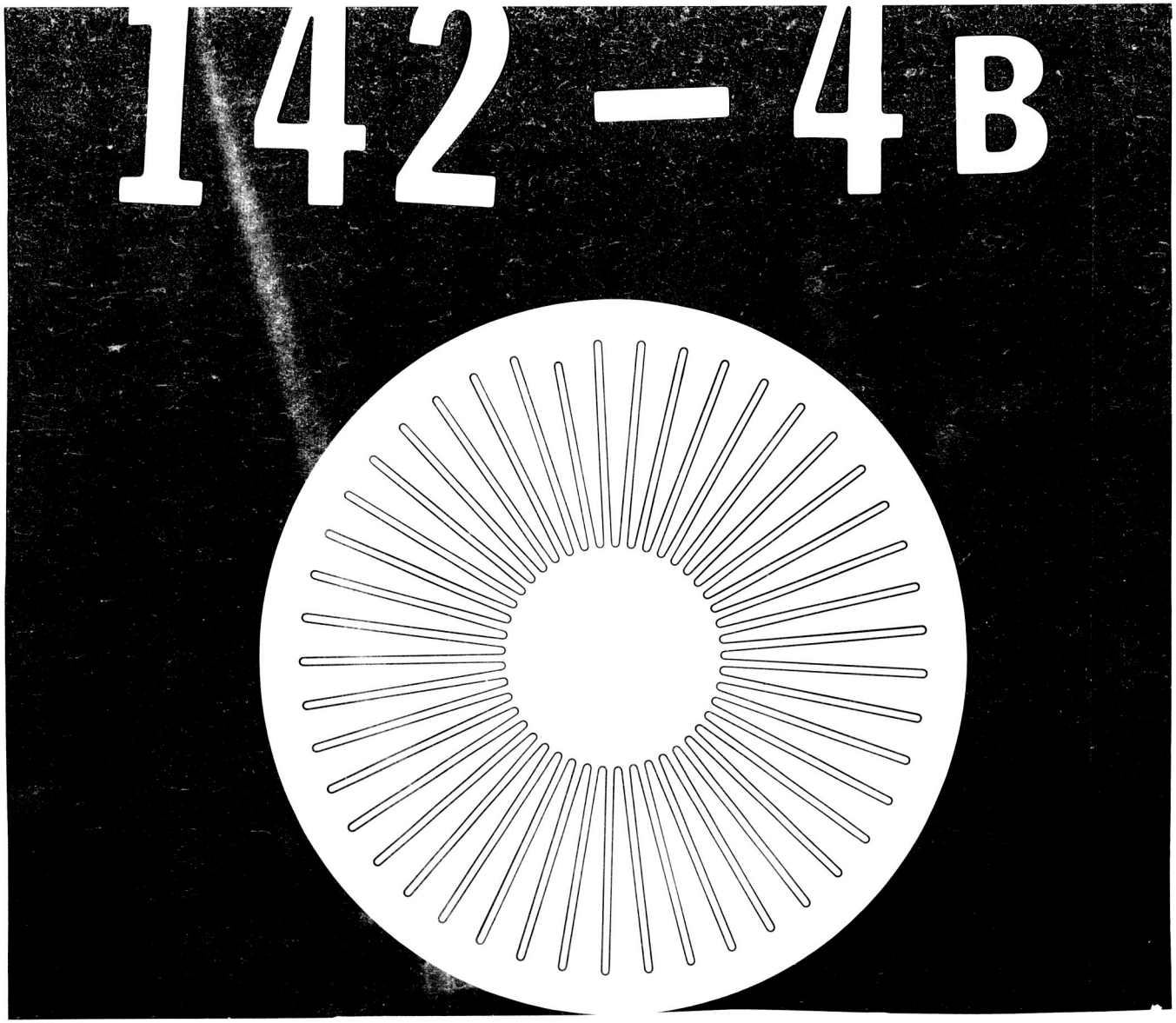


Figure 24

Inverse Emitter Mask
100A Transistor

142-10

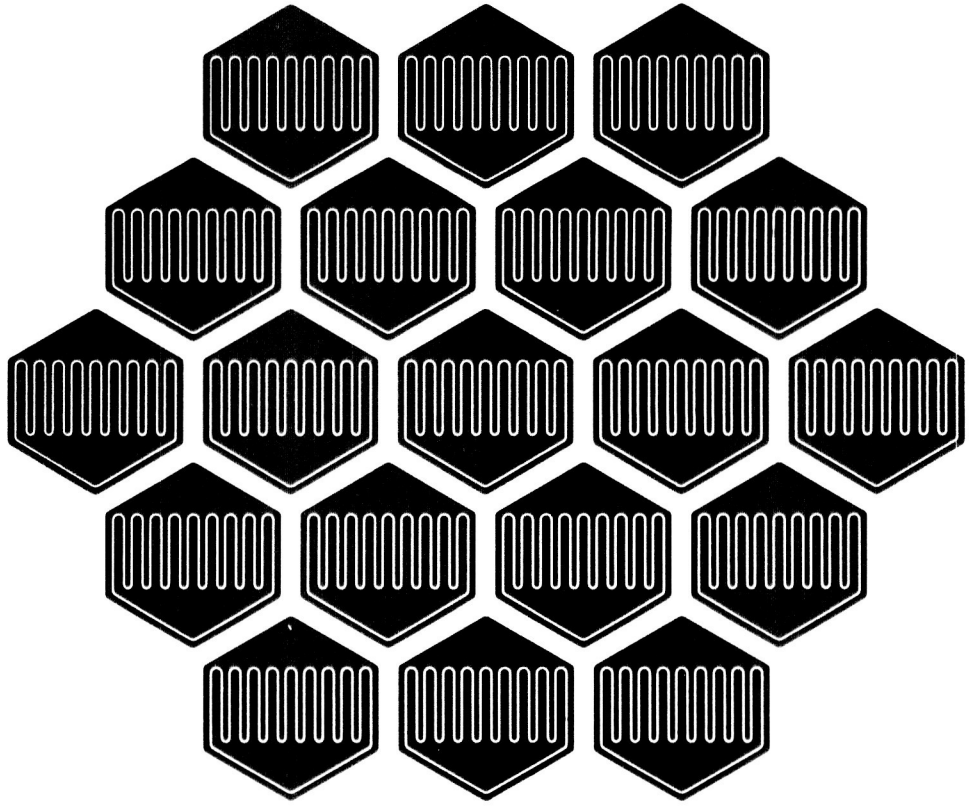


Figure 25

Inverse Emitter Mask
10A Transistor

142-7

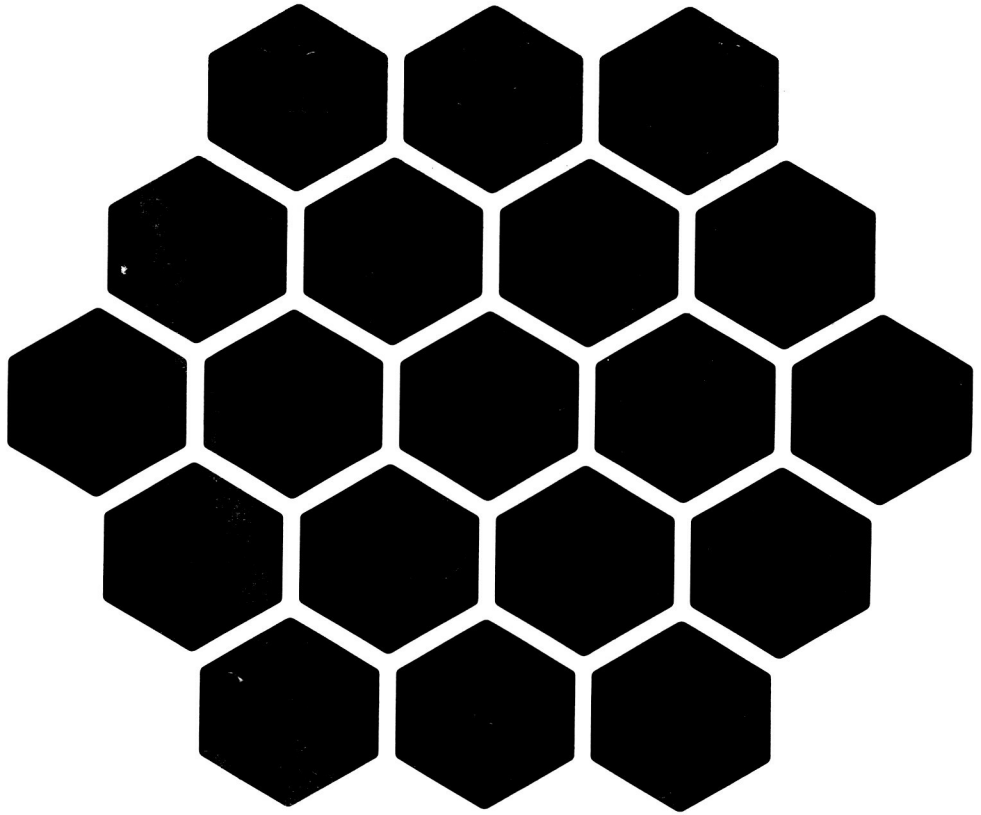


Figure 26

Mesa Mask
10A Transistor

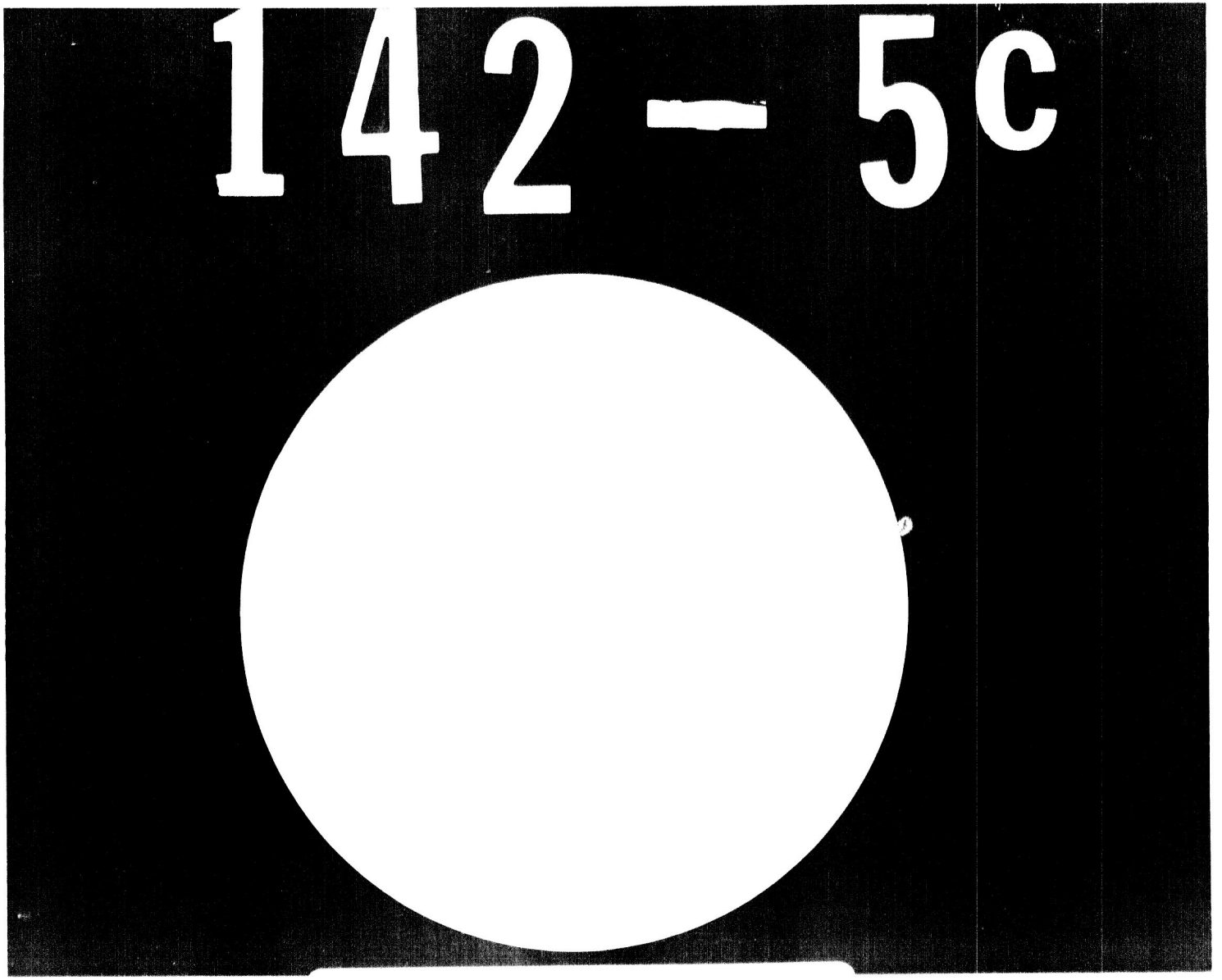


Figure 27

Mesa Mask
100A Transistor

V. ENCAPSULATION

A. REVIEW OF EARLIER VERSION

The encapsulation of this transistor went through several modifications. It was mentioned in Section II-A that the emitter geometry first considered was a nineteen-module structure on a 1-inch diameter wafer. A critical analysis of the banding of twenty individual wires to the required 10 modules was expected to be almost impossible, especially when the threading of these wires through small holes simultaneously was considered in conjunction with the assembly problem.

Because of the severity of this problem, the emitter geometry was redesigned. This design permitted a much simplified contacting procedure utilizing the compression bond technique which was being successfully used on other high power devices. The emitter contact was a ring structure and the base contact was a dot structure. An insulating pressure pad was used to distribute the pressure over the finger structure between the emitter contacting ring and the base contacting dot.

The possibility of nonplanarity of the transistor element suggested some modification of the encapsulation system. The emitter contact was a circular silver ring and the base was a circular silver disc. This system also showed several weaknesses. The inspection of the transistor after disassembly indicated the emitter ring was causing surface damage on the contact and where the pressure was excessive. It was also observed that the emitter ring was not making contact with the emitter area uniformly. Because of these drawbacks, the second version was further modified. And the final version was adopted. The encapsulation details of the final version are given in this section.

B. CUSHIONING MATERIAL

It has long been recognized that excessive localized stresses on a compression bonded device will cause downgrading or even complete failure of the device. Due to the narrow emitter contacting surface, the subject device was especially subject to excessive localized stresses.

In order to spread the compression force required for encapsulation over the whole surface of the device, a search was made for a material with mechanical, electrical and thermal characteristics suitable for intimate contact with the surface of the device. One material that was readily available and uniquely suited to the requirements was Teflon*, type TFE (polytetrafluorethylene).

The literature[12] shows that parts made of TFE deform in time at a decreasing rate. This property can best be explained by the concept of "Apparent Modules of Elasticity." This concept takes into account the initial deformation for an applied stress plus the amount of deformation that occurs with time. At a given compressive force and temperature the initial deformation of TFE occurs within the first few hours. The deformation then levels off to a point where it is negligible.

The electrical properties of TFE in the required thickness far exceed the electrical characteristics of the device. Sleeving of Teflon is already being used as lead wire insulation inside many of the Westinghouse transistors and controlled rectifiers.

The above-mentioned literature shows that TFE is useful from -267°C to +260°C. This far exceeds the rating of the subject device. Since TFE is inert to almost all chemical reactants it is an ideal substance to mate to the entire surface of the device.

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* Registered trademark of E. I. DuPont de Nemours and Company.

(12) Teflon Fluorocarbon Resins, Mechanical Design Data, Plastic Dept., E. I. DuPont de Nemours and Company, Wilmington, Delaware 19898, Materials in Design Engineering, Feb. 1964.

C. DESIGN OF COMPRESSION ELEMENTS

The design of the compression elements of the subject device is very similar to that of the Type 221 SCR which has proven very successful.

1. Emitter. Figure 28 shows the components of the emitter compression. Following is a brief description of each:

Emitter Lead(6) - Applies direct force to the emitter contact. The base compression elements are contained within the tube leading to the ceramic-metal seal.

Small Thrust Washer(7) - Provides a solid, flat base for the mica insulation. It is chamfered on one side to fit over the brazed fillet between the washer and the tube of the emitter lead.

Mica Insulation(8) - Insulates the emitter from the collector portions of the case. Also serves as the locator to properly center the emitter lead.

Large Thrust Washer(9) - This washer serves as a bearing surface between the mica washer and the Belleville springs.

Belleville Springs(10) - Maintains the force applied during pre-encapsulation. Used in a series of three in order to gain maximum deflection. This ensures that the highest possible force is maintained as the emitter contact conforms to the surface of the device. Maximum force maintained - 900 lbs.

Large Thrust Washer(11) - This lies on top of the bearing surface of the Belleville springs.

Internal Nut(13) - After force has been applied during pre-encapsulation, the nut is screwed down against the top thrust washer. When force is released, the Belleville springs are maintained in a deflected state.

2. Base. Figure 29 is a cross section of the base compression elements. Following is a brief description of each:

Nail Head Lead Wire[21] - This contacts the base region of the basic fusion and leads to the ceramic-metal seal.

Teflon Locator[15] - This was fully described during the discussion of the base contact element.

Mica Insulation[18] - Distributes the force of the coil spring over the top surface of the locator.

Coil Spring[19] - Provides the force required to maintain contact to the basic fusion when force is applied to the emitter compression assembly.

Base Lead Insulation[16] - Insulates the lead wire from the emitter and collector regions of the assembly.

Plug[22] - Forced into the top of the emitter tube to hold the base components in place.

The above components are preassembled in the emitter lead tube prior to the pre-encapsulation procedure.

D. DESIGN OF CONTACTING ELEMENTS

The contacting elements were designed so that no changes in external outline would be required. Figure 28 shows the completed device in cross section.

1. Emitter. Figure 30 shows the details of the emitter contact. It consists of a Teflon washer with a thin layer of silver foil formed around it to conform with the emitter contacting surface of the basic device. The thickness of the Teflon washer was designed so that the stress-strain characteristics would allow it to flow and conform to the emitter lead and device surface, yet not so great that it would push the emitter contact area from the surface of the device. The silver foil was fashioned to allow cold flow of the Teflon. This can be recognized as the expansion arch in Figure 30.

2. Base Contact. The basic contact element (Figure 29) consists of a nail head silver wire and Teflon locator. An important feature of the Teflon locator is the reverse chamfer at the contacting surface. This feature allows for the cold flow of the emitter contact under pressure, which in turn locks the base in place. The Teflon locator serves another important function in centering the emitter contact on the surface of the basic fusion.

In the first emitter contacts the silver was notched and formed around the Teflon cushioning pad by hand. It was very difficult to align the contacting area accurately and form the expansion arch. Tooling was designed and the remaining contacts were made by a multiple punch and die method. This method left wrinkles on the contacting surface, but it was found that these wrinkles did not adversely affect the characteristics of the device.

3. Collector. It was very important that in designing the collector contact, to keep in mind that it is through this contact that the heat generated within the basic fusion flows to be dissipated in the base and heat sink. This required that the molybdenum mounting disc of the basic fusion and the base be in intimate contact. To enhance the initimate contact between the basic fusion and the base, a dead soft silver disc was placed between them. The purpose of this disc was to fill as many voids (due to lack of flatness and surface finish) as possible in both the molybdenum mounting disc and pedestal surface.

Upon examining the foil after disassembly, the imprint of the molybdenum and the base surface irregularities were clearly visible; indicating that the silver foil was performing as intended.

E. PRE-ENCAPSULATION PROCEDURE

All components except the mica insulators are thoroughly degreased in trichloroethylene. The mica is baked and stored in vacuum at 150°C for 12 hours prior to assembly.

1. Base-Emitter Sub-Assembly

a. The small thrust washer is placed over the top of the emitter lead and seated on the top surface of the emitter lead.

b. Two mica insulating washers are placed over the emitter lead tube and seated on the small thrust washer.

c. The emitter lead is inverted and the spring placed in the emitter lead tube and set against the plug.

d. Two mica insulating discs are seated on the spring.

e. A nail head lead wire is placed through the Teflon locator and set against the bottom of the locator.

f. A piece of gate lead insulation is placed over the lead wire and in the counterbore of the locator.

g. The lead wire and Teflon locator are inserted in the emitter tube and the wire and insulation brought through the slot in the tube as the locator is seated against the mica.

h. The emitter lead is then turned right side up and the large thrust washer (.040" thick) is placed over the emitter tube and base lead wire and on top of the mica insulator.

i. Three Belleville springs are then seated on the large thrust washer (.040") in series with the first washer, concave side up.

j. The large thrust washer (.060" thick) is then seated on the Belleville springs.

k. The inner nut is then placed on the large thrust washer (.060") with the flat side down.

2. Pre-Encapsulation

a. A piece of silver foil is placed in the inner case and set on the base.

b. The basic fusion is put into the inner case and seated on the silver foil, with the molybdenum side down.

c. The emitter contact is centered on the surface of the basic fusion.

d. The base-emitter sub-assembly is placed in the inner case. The Teflon locator is guided into the inside diameter of the emitter contact and pressed down as the slack on the inner nut is taken up.

e. The sub-assembly is then placed on a press and force is applied to the large thrust washer (.060") to compress the Belleville springs (at the same time the inner nut is being tightened). This step is repeated three times to overcome as much friction as possible.

The units were then ready for the final encapsulation procedure.

F. FINAL ENCAPSULATION PROCEDURE

For the final encapsulation procedure, the parts involved were prepared as follows. The ceramic-metal seal was leak tested, degreased, and baked in vacuum at 175°C for 4 hours. The molecular sieve was baked at least 16 hours in vacuum at 300°C. They were then stored in vacuum at 150°C. The pre-encapsulated assembly was baked in air at 175°C for 4 hours prior to the final encapsulation.

All components in this section are shown in Figure 28 .

Procedure

1. The molecular sieve was placed over the emitter tube and seated, inside the inner nut, on the large thrust washer .060" th.

2. The base lead wire was guided through the base lead connector as the ceramic-metal seal was placed over the inner case and seated on the weld ring.

3. The base lead wire was pinch welded inside the connector.

4. The ceramic-metal seal was resistance welded to insure hermeticity of the assembly.

5. The emitter lead connector was then crimped in place.

6. The device was leak tested and plated with nickel.

The final encapsulation was then complete and the devices were ready for final electrical testing.

G. FORCE VS. THERMAL IMPEDANCE

In order to dissipate the heat generated in a power device, it is imperative that the basic fusion be in intimate contact with the base. In the subject device this intimate contact is achieved by means of the compression bond encapsulation technique developed by Westinghouse for high power silicon controlled rectifiers. Since the Type 142 is one of the first power transistors to use this technique, little data was available as to the amount of force which would be required to achieve and maintain a low thermal impedance contact between the basic fusion and the base.

Engineering data recorded from past experience on the 250 amp Type 221 silicon controlled rectifier indicated that the thermal impedance decreased as the force increased. Figure 31 shows the results of an experiment conducted on several Type 221 SCR's. It can be seen that there is a definite decrease in thermal impedance of all the devices as the force is applied up to about 750 lbs. From then on, the rate of decrease begins to level off to a very gradual slope. From this data, it was reasonable to assume that at least 900 lbs. of force would be required to achieve the intimate contact needed to carry off the heat generated in the basic fusion. The final test results on the subject device shows that the thermal impedance is well within the specified limits.

WESTINGHOUSE ELECTRIC CORPORATION

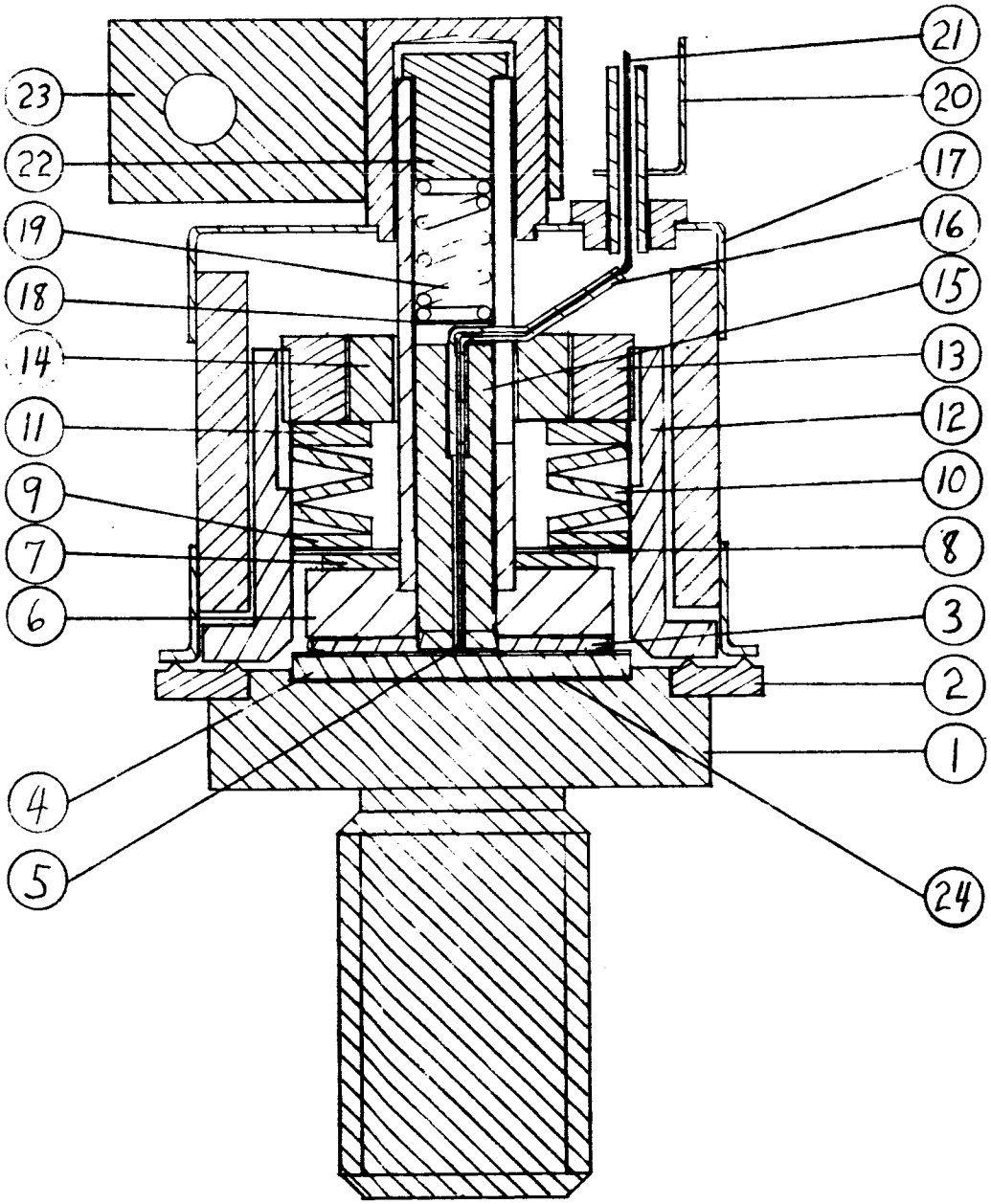


Figure 28

Cross Section of Encapsulated Device

TYPE 142 100 AMP TRANSISTOR	SCALE 2"=1"	E.D.Sk. A 310771
REFER TO ED SK A 310772 FOR DESCRIPTION	J. STEINMETZ	

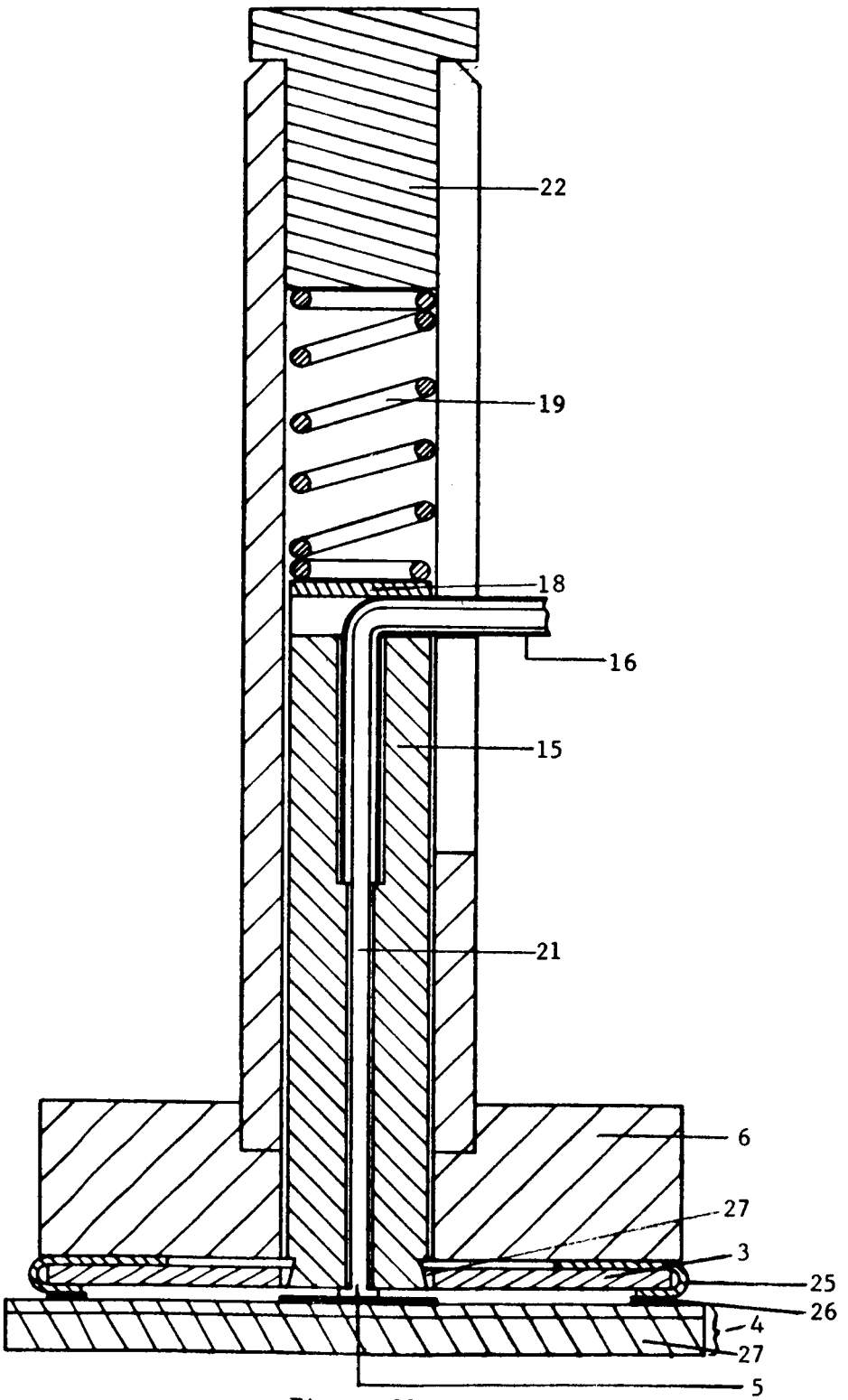


Figure 29

Base Compression Elements

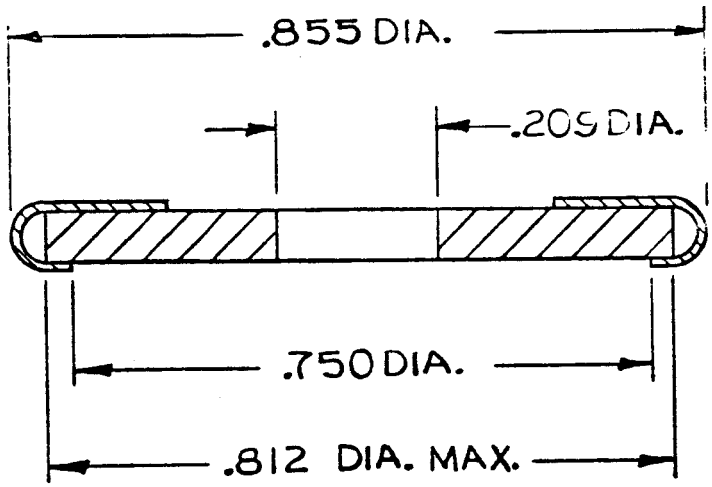


Figure 30

Details of Emitter Contact

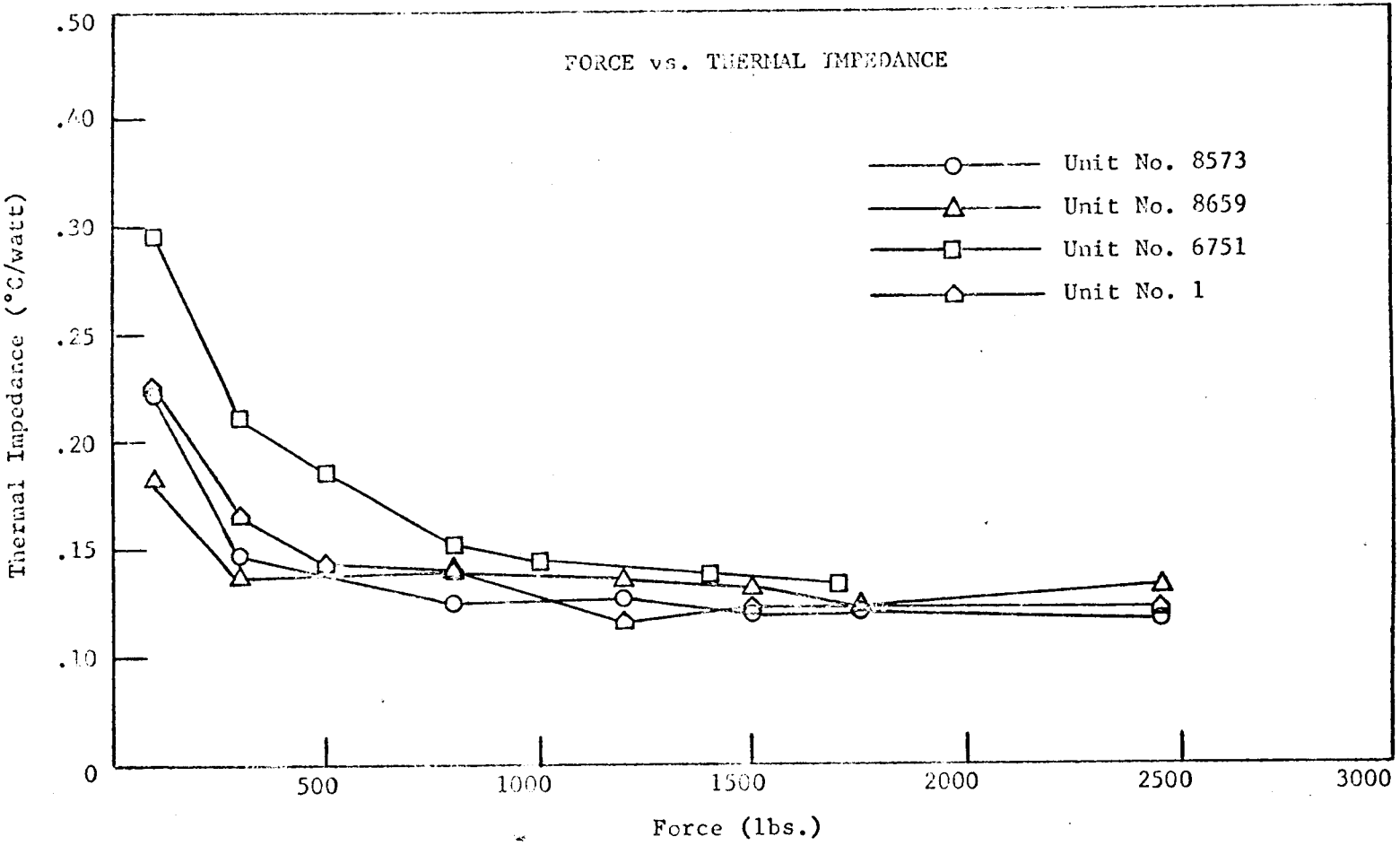


Figure 31

Force vs. Thermal Impedance

VI. TEST RESULTS

A. ELECTRICAL TESTS

Electrical tests were performed at various stages of the fabrication.

1. Voltage. In order to test the voltage capability of the epitaxial junction, the slices were sandblasted to expose the collector-base junction. The collector-base voltage was measured using a Tektronix curve tracer 575. A special test fixture was made to test the slices by making contacts over the active area of the slices. The results are shown in Table VII. Three of these slices were etched into small mesas using the mask shown in Figure 26 and the collector-base voltage was again measured using the Tektronix curve tracer. The results are shown in Table VIII and photographs of the breakdown characteristics are shown in Figure 32. All the mesas exhibit high breakdown voltage with rather low leakage. The voltage distribution is reasonably regular showing a pattern quite expectable with minor material variation.

The voltage capability of the 100A transistor was tested before encapsulation and the units that showed poor voltages were rejected. The transistors that showed good voltages were encapsulated and the electrical tests were again performed to insure the encapsulation step had not degraded the units. The result of the voltage tests before and after encapsulation are given in Table IX. The electrical circuits used to measure the collector-emitter breakdown voltage (V_{CEO}) and the sustaining voltages are given in Figures 33 and 34.

Voltage measurements were also made at different temperatures. The units were stacked in a temperature controlled oven and the voltage reading was taken at 125°C, 150°C and 175°C. The results are shown in Table X.

2. Saturation Voltage. The saturation voltages were measured by using a Dynatron pulse tester. The circuit used to measure the collector-emitter saturation voltage, $V_{CE(sat)}$, and the base-emitter saturation voltage, $V_{BE(sat)}$, is shown in Figure 35 . A pulse width of 300μsec. and a duty cycle <2% was used for the test. In the common emitter circuit, the specified I_B (10 ampere) was applied. The collector current was driven up to 100A and the $V_{CE(sat)}$ and $V_{BE(sat)}$ were read off directly. The results of the tests given in Table XI .

3. Current Gain. The current transfer ratio (h_{FE}) at low current level was tested with a Tektronix curve tracer and the corresponding reading at high current level was made with a Dynatron pulse tester. The electrical circuit used is shown in Figure 36. In the common-emitter circuit, the specified voltage (4V) was applied between the collector and the emitter; and then the specified collector current of 100A was applied. The base current was then measured and the forward current transfer ratio was calculated using

$$h_{FE} = \frac{I_C}{I_B} .$$

The results are shown in Table XI. The current transfer ratio as a function of collector current is given in Table XI for a number of typical units. Figure 37 shows h_{FE} of three transistors as a function of collector current. It is seen from the figure that h_{FE} is fairly uniform over the operating range of collector current; this is essential to minimize the switching characteristics.

4. Switching Tests. The switching tests of the transistors were performed using the circuit shown in Figure 38 . The test conditions are given in Figure 39. The typical display for the switching test is shown in Figure 39 . The device was mounted on an appropriate heat sink. $I_{B(on)}$ and $I_{B(off)}$ was measured for each test, since I_B in each case might vary with input impedance. V_{CE} was applied until I_C was measured to be 20A.

Because of the limitation of the circuit, the switching measurement was conducted only up to 20A. The results of the tests are given in Table XII.

B. ENVIRONMENTAL TESTS

Several units were subjected to temperature cycling from -65°C to +200°C. The results for two typical units before and after the temperature cycling tests are shown in Table XIII.

The transistors were also subjected to shock and centrifuge tests in all three planes. The equipment used for the test is shown in Figure 40 and the results are given in Table XIII.

The vibration test was done on the apparatus shown in Figure 41. The test was done at 20G's with 100 to 2000cps in all three planes. The results of the tests are also shown in Table XIII.

Two transistors were stored in a 200°C oven for 1282 hours. The electrical characteristics of the transistors were taken at several intervals and are shown in Table XIV.

C. THERMAL TEST

Thermal measurements were made with the circuit shown in Figure 42 . This is the circuit presently used in evaluating the standard line of Westinghouse power transistors. The measurement method used the forward-biased collector-base voltage at a constant current level as the temperature sensitive parameter (TSP). With the device at an elevated temperature the TSP was measured with no power dissipation in the device. The case temperature was then lowered a known amount and power was dissipated until the TSP measured the same as before. The TSP was measured by means of mercury relays which interrupt the power and connect the measurement oscilloscope to the circuit. The results of the thermal tests of four typical units are shown in Table XV .

The electrical characteristics of the five final transistors delivered to NASA are shown in Tables XVI and XVII.

TABLE VII

Results of Collector-Base Voltage Test

Unit No.	V_{CB} V/ma
2-1	180/35
1-2	180/35
4-3	100/50
5-4	150/50
4-5	150/50
2-6	200/25
2-7	180/50
5-8	190/25
3-9	20/50
5-10	80/50
3-11	150/50

TABLE VIII

Voltage Capability of Epitaxially Grown Diodes (small area mesa)

Slice No.	Mesa No.	V_{CB}/1ma	Mesa No.	V_{CB}/1ma
1	1	180	11	180
	2	180	12	180
	3	180	13	160
	4	180	14	170
	5	170	15	180
	6	180	16	180
	7	180	17	160
	8	160	18	170
	9	160	19	170
	10	180		
		140 volts at .02ma		
2	1	160	11	160
	2	160	12	160
	3	160	13	160
	4	160	14	160
	5	160	15	160
	6	170	16	160
	7	170	17	160
	8	160	18	160
	9	160	19	160
	10	160		
		140 volts at .03ma		
3	1	180	11	180
	2	170	12	170
	3	180	13	180
	4	180	14	180
	5	170	15	180
	6	180	16	170
	7	180	17	180
	8	180	18	170
	9	180	19	180
	10	180		
		140 volts at .03ma		

TABLE IX

Voltages Before and After Encapsulation

Unit No.	V_{CE}	I_{CE}	V_{CB}	I_{CB}	V_{EB}	I_{EB}	V_{BE}	I_{BE}
PRE-ENCAPSULATION								
118-1	100	15	100	10	.7	5	14	50
118-2	45	50	50	35	.8	5	14	60
119-1	100	50	100	40	.8	5	13	10
119-2	15	100	35	100	.8	5	14	10
119-3	100	5	100	4	.9	5	14	10
119-4	100	50	100	15	.9	10	15	20
119-5	25	200	40	100	.8	5	16	60
120-1	20	250	45	250	12	100		
120-2	200	40	250	20	12	100		
120-3	185	60	130	35	13	200		
122-1	150	12	150	10	11	100		
122-2	25	50	65	50	18	50		
122-3	.3	100	12	50	12	50		
122-4	50	16	60	10	12	25		
123-1	14	100	15	100	11	100		
123-2	14	100	15	100	11	100		
123-3	55	50	100	25	15	25		
123-4	50	45	50	28	10.5	50		
123-5	70	30	100	15	4.5	25		
125-1	140	20	140	15	5	200		
125-2	23	200	25	60	12	100		
125-3	130	30	150	30	12	200		
125-4	65	100	100	75	10.5	50		
125-5	120	15	150	10	11	25		
POST-ENCAPSULATION								
118-1	100	15	100	10	.8	5	15	40
118-2	50	20	50	15	.9	5	15	200
119-1	100	50	100	40	.8	5	14	20
119-3	100	5	100	5				
119-4	95	40	100	60				
120-1	20	250	45	250	12	100		
120-2	160	7	170	7	12	40		
120-3	160	35	180	35	13	100		
120-4	135	35	140	40	13	100		

(continued on next page)

TABLE IX (continued)

Unit No.	V_{CE}	I_{CE}	V_{CB}	I_{CB}	V_{EB}	I_{EB}	V_{BE}	I_{BE}
122-1	50	12	150	10	11.5	100		
122-2	30	100	70	50	18.5	50		
122-4	55	18	65	12	12.5	50		
123-1	35	100	35	25	8	100		
123-3	100	150	150	60	16	50		
123-4	150	140	160	80	13.5	100		
123-5	140	125	150	30	15	25		
125-1	140	20	140	15	5	200		
125-2	25	200	25	60	11.5	100		
125-3	150	40	150	30	11.5	200		
125-4	130	200	135	120	10.5	50		
125-5	140	30	150	10	11.5	25		

TABLE X

Electrical Characteristics at Different Temperatures

Unit No.	V_{EBO} V/ma	V_{CEO} V/ma	V_{CBO} V/ma	h_{FE} at 20A	$V_{CE(sat)}$ at 40A	V_{EBO} V/ma	V_{CEO} V/ma	V_{CBO} V/ma	h_{FE} at 20A	$V_{CE(sat)}$ at 40A
118-1	10/30	170/30	260/30	21	.35	23/30	43/30	155/30	28.5	.6
119-1	10/30	50/30	70/30	19	.38	27/30	20/30	98/30	33.5	.6
119-3	10/30	200/10	200/10	21	.25	---	160/30	170/30	33.2	.6
119-4	11/30	80/30	80/30	15	.36	---	85/30	82/30	28.5	.6
116-2	12/30	9/30	50/30	12	.45	26/30	8/30	65/30	15.3	.6
116-3	12/30	20/30	22/30	12	.4	---	20/30	23/30	18	.7
117-1	9/30	5/30	10/30	20	.5	15/30	3/30	20/30	33.2	.8
117-2	5/30	42/30	48/30	21.2	.5	5/30	40/30	70/30	40	.8
120-2	10/30	210/30	220/30	8	.8	10/7	170/30	175/30	11.8	1.6
120-3	9/30	140/30	185/30	10.5	.8	11/30	30/30	150/30	17	1.7

TABLE XI

Saturation Voltage and Current Gain

Unit No.	$V_{CE(sat)}$ V at 80A	$V_{BE(sat)}$ V at 80A	h_{FE} 20A	40A	60A	80A	100A
116-2	.9	1.2	11.8	10.5	10.3	10.2	--
116-3	.8	1.35	11.8	11.1	11	10.7	--
117-1	1.1	1.25	30	20	18.8	16	11
117-2	1.0	1.25	21	22.2	19.5	17.5	10.8
118-1	.8	1.1	21	18.5	17.6	15	10
119-1	.75	1.1	19	17.4	15.8	14.2	12
119-3	.5	1.1	21	21	19.3	17.6	13.3
119-4	.75	1.1	14.8	17.3	17	16.2	11.6
122-2	.8	1.4	25	22.2	20	17	13.2
122-4	.4	1.1	18.2	17.2	16	15	13
123-3	1.7	2.6	50	42.5	30	24.3	18
123-5	.9	1.7	44.5	36.5	27.3	22.8	17
126-1	.34	--	13.3	13.2	12.5	12.3	11
126-2	.57	1.2	17.6	16.7	16	15	13
126-4	.67	1.11	13.6	13.5	12.5	12	10

TABLE XII

Switching Characteristics

Unit No.	t_d μs	t_r μs	t_{d+r} μs	t_s μs	t_f μs	t_{s+f} μs
122-2	.5	1.5	2	.45	.15	.6
123-1	.5	1.0	1.5	.35	.1	.45
123-3	.5	2.5	3.0	.4	.2	.6
123-4	.55	.95	1.5	.4	.15	.55
123-5	.5	1.5	2.0	.5	.15	.65
125-1	.5	1.5	2.0	.3	.15	.45
125-4	.6	1.4	2.0	.2	.15	.35
125-5	.55	.95	1.5	.45	.05	.50
126-2	.5	1.2	1.7	.3	.1	.4

TABLE XIII

Environmental Tests

Unit No.	volt/ma	volt/ma	volt/ma	volt/ma	β
BEFORE TESTS					
Post Encapsulated and Plated					
111-1	20/120	30/60	.7/250	14/250	33/10A
111-2	3/250	16/250	.7/250	13/250	40/10A
114-1	7.5/250	7/250	.7/250	1.2/250	8/10A
114-2	35/250	55/250	.7/250	6/250	25/10A
AFTER TESTS					
Post Temperature Cycling Tests					
114-1	7/250	8/250	.7/250	3/250	8/10A
114-2	35/200	55/250	.8/250	7/250	25/10A
Post Vibration and Centrifugal Tests					
111-1	6/250	13.8/250	.6/5-.85/250	15/140	33/10A
111-2	3.2/250	16.5/250	.7/250	13/250	20/10A

Centrifugal = 500G's X, Y and Z Planes

Vibration = 20G's 100-200cps X, Y and Z Planes

TABLE XIV

Storage Life (200°C)

Unit No.	V_{EB} 10ma	V_{CB} 10ma	V_{CE} 10ma	Hours	β 2A	β 5A	β 10A	$V_{CE(sat)}$ 5A	$V_{CE(sat)}$ 10A
37-10	1.8V	37V	18.2	16	14	10	7.5	.7V	1.2V
37-9	3.7	135V/50ma	110V/10ma		2.5	4	-	.8V	-
37-10	1.8	38	18		13	10	7.5	.6V	1.3V
37-9	3.8	135V/50ma	110	40	2.5	4	-	.9V	-
37-10	1.8	39	18		12	10	7.5	.6V	1.3V
37-9	3.8	110V	130V	184	2.5	4	-	.9	-
37-10	1.8	20V	43V		13	10	8.2	.7V	1.4
37-9	3.8	110V	110V	496	2.5	2.5	-	.9	-
37-10	2.2	37	18	1282	13	11	7.5	.8	1.42
37-9	2.0	115	110		2.5	2.2	-	1.0	-

TABLE XV

Thermal Tests

Unit No.	T_J °C	T_S °C	ΔT °C	W watts	θ_{J-C} °C/watt
120-3	52	33	19	57	0.333
120-2	63	41	22	63.5	0.347
125-4	50	34	16	56	0.286
125-1	52	38	14	62.5	0.224

TABLE XVI

Electrical Characteristics of the Final Devices

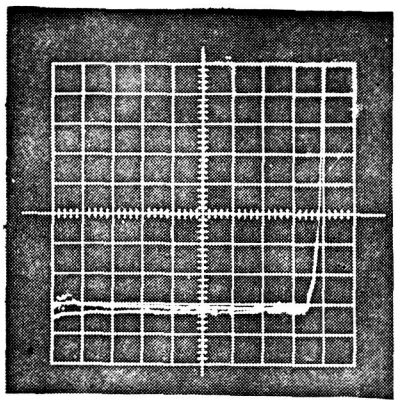
Unit No.	V_{EBO} volt/ma	V_{CEO} volt/ma	V_{CEX} volt/ma	V_{CBO} volt/ma	I_B = 10A $V_{CE(sat)}$ 40A	$V_{CE(sat)}$ 80A	$V_{BE(sat)}$ 40A	$V_{BE(sat)}$ 80A	t_{on}(μsec)	t_{off}(μsec)	h_{FE} 10	20	40	60	80	100 Amps
118-1	10/40	170/30	220/30	260/30	-	.48	-	1.1	1.3	.7	22	21	18	17.6	15.5	10
119-1	14/20	110/50	110/50	110/60	-	.75	-	1.1	1.7	.7	20	19	17.5	15.8	14.5	12.5
119-3	1/100	200/10	200/5	200/10	-	.5	-	1.1	1.5	1.0	27	21	21	19.5	17.8	13.5
120-3	10/75	140/30	165/30	185/30	-	1.2	-	1.35	1.7	.6	10	10.5	9.5	8.8	8.0	-
125-3	11.5/200	150/30	150/20	150/40	.5	1.5	1.8	2.3	1.5	.36	7	8.5	8	7.5	-	-
125-5	11.5/25	150/40	150/30	150/10	.5	-	1.3	1.6	1.5	.5	9.5	11	10.5	9.8	8.8	-

TABLE XVII

Electrical Characteristics of the Final Devices

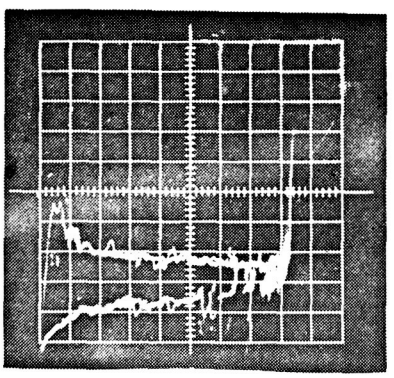
Hot Test (150°C)

Unit No.	V_{EBO}	V_{CEO}	V_{CBO}	10A h_{FE}
119-3	15/30	150/10	150/5	40
118-1	15/60	75/200	150/45	28
119-1	15/50	145/60	165/55	28
125-5	13.5/100	150/14	160/8	16
125-3	13/200	150/20	150/15	14
120-3	14/100	150/30	160/20	16



Vertical 0.1ma/Division
Horizontal 20V/Division

Breakdown Voltage of a Good Small-Area Mesa (Group C - Slice #2, Unit #6)



Vertical 0.01ma/Division
Horizontal 20V/Division

Breakdown Voltage of a Good Small-Area Mesa (Group C - Slice #2, Unit #6)

Figure 32

Breakdown Characteristics

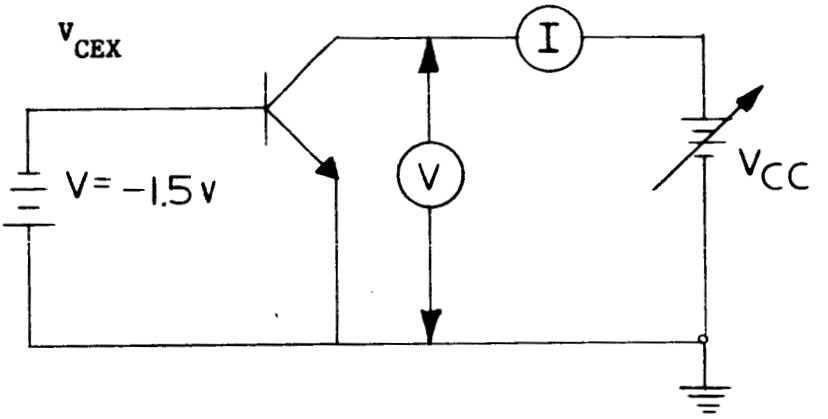


Figure 33

Collector-Emitter Sustaining Voltage Test Circuit

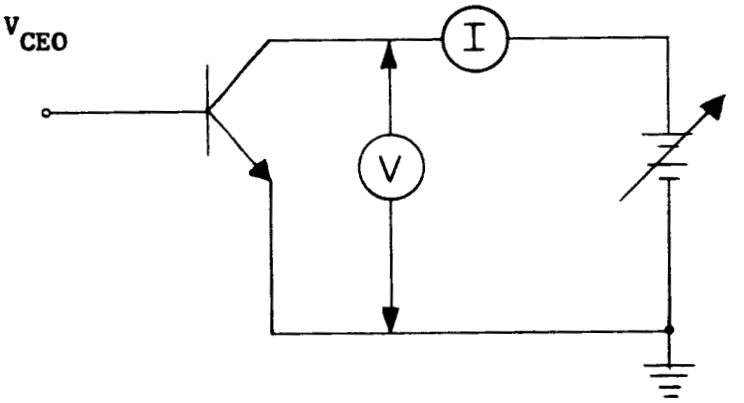


Figure 34

Collector-Emitter Breakdown Voltage

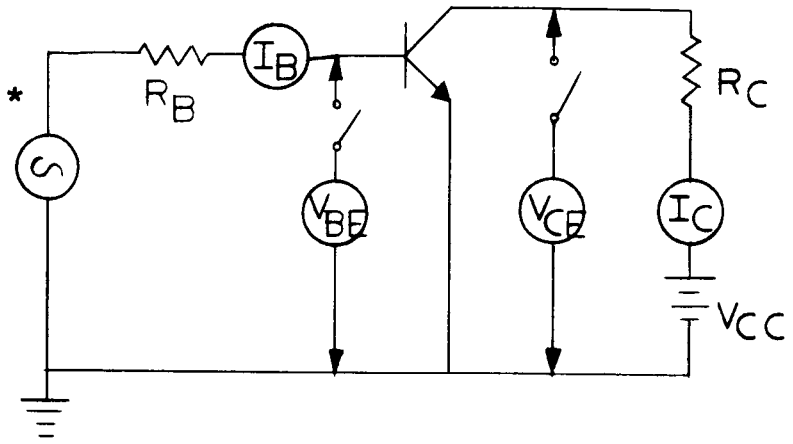


Figure 35

$V_{CE(sat)}$ and $V_{BE(sat)}$ Test Circuit

*Pulse test, duty cycle $\leq$ 2%, pulse width = 300μsec. In the common emitter circuit, the specified I_B (2X overdrive) is applied, the collector supplied is driven until 100A is across the collector-emitter. $V_{CE(sat)}$ and $V_{BE(sat)}$ is a direct reading.

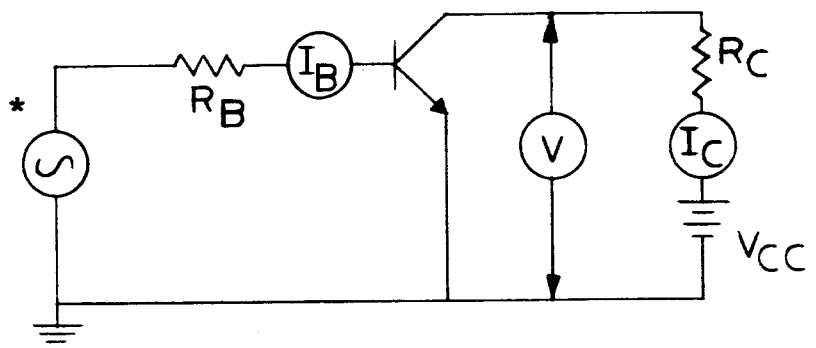


Figure 36

Current Transfer Ratio Test Circuit

*Pulse test, duty cycle $\leq$ 2%, pulse width = 300μsec. In the common emitter circuit, the specified voltage (4V) is applied between the collector and emitter, the specified collector current (1-100A) is applied. The base current is then measured. The forward current transfer ratio is calculated as $h_{FE} = \frac{I_C}{I_B}$.

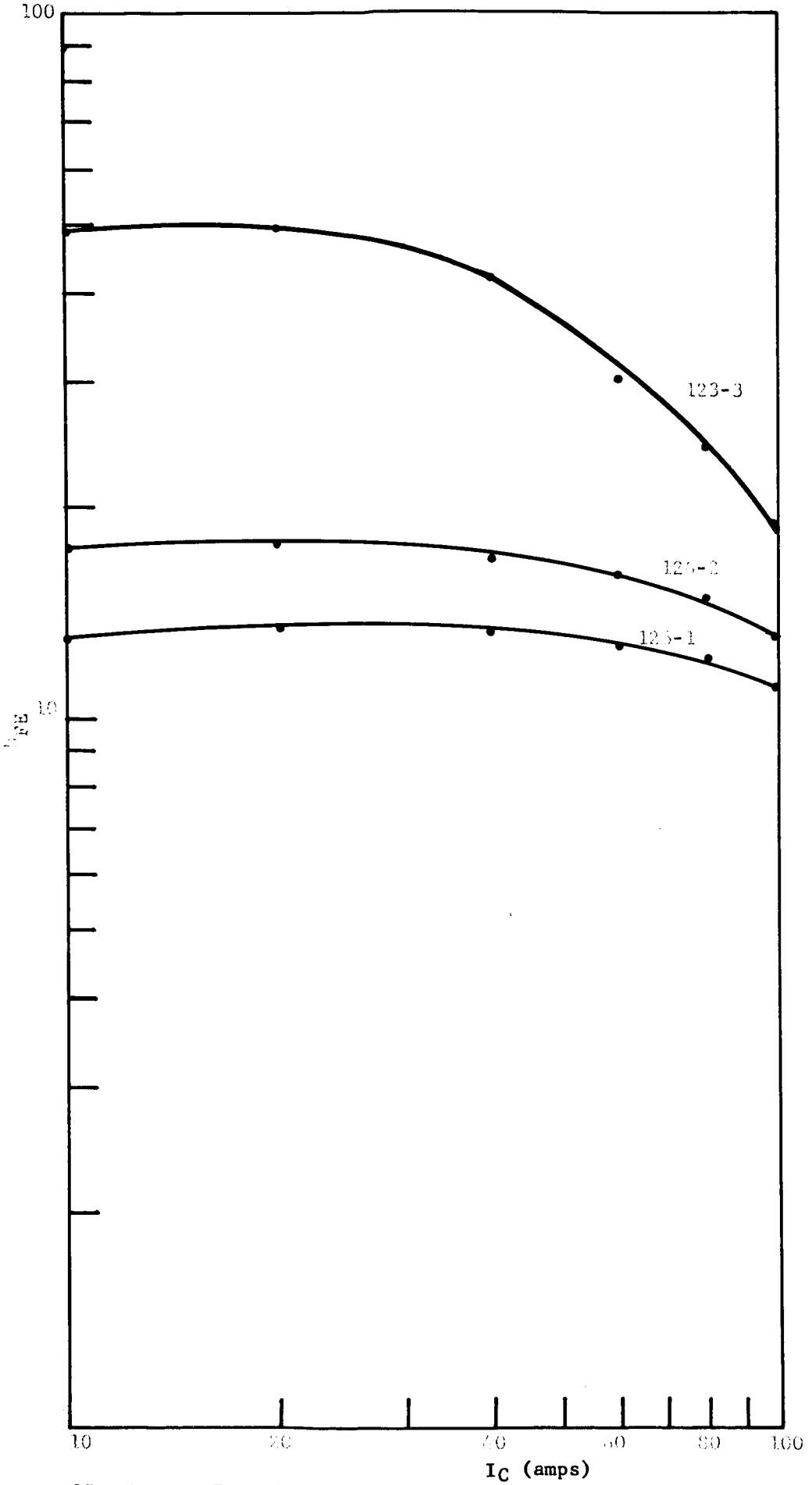
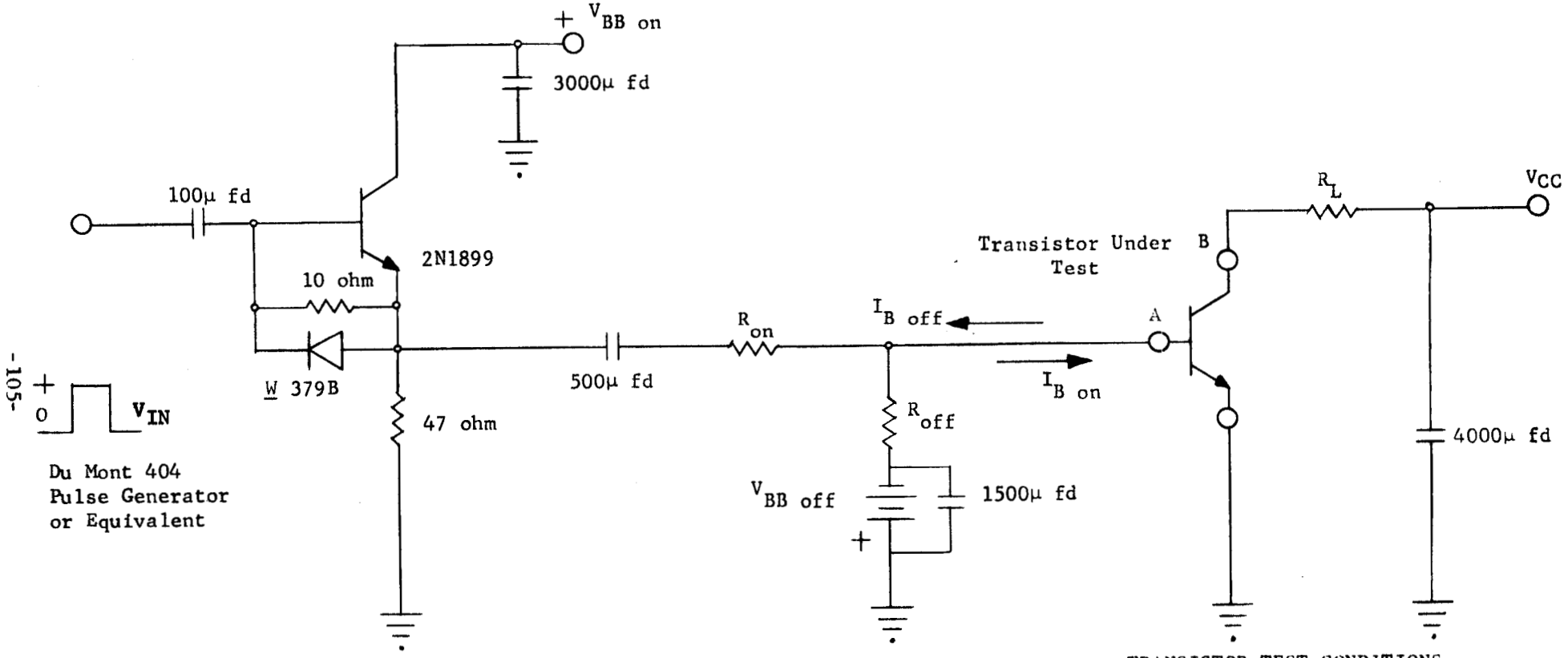


Figure 37: h_{FE} as Function of Collector Current for Three Transistors

SWITCHING TEST CIRCUIT FOR TRANSISTORS



I_B(ON) and I_B(OFF) measured at Point A with Tektronix Type 131 Current Probe Amp.

I_C measured at Point B with same Probe.

TRANSISTOR TEST CONDITIONS

V_{CC}	=	12V	Input Pulse
R_L	=	.55 ohm	cps rep.rat = 10 cps
I_C	=	20A	μ sec pulse width=20μsec
I_B on	=	3A	
I_B off	=	3A	
R on	=	3.9 ohm	
R off	=	6.8 ohm	
V_{BB} on	=	40V	
V_{BB} off	=	15V	

Figure 38

Switching Test Circuit

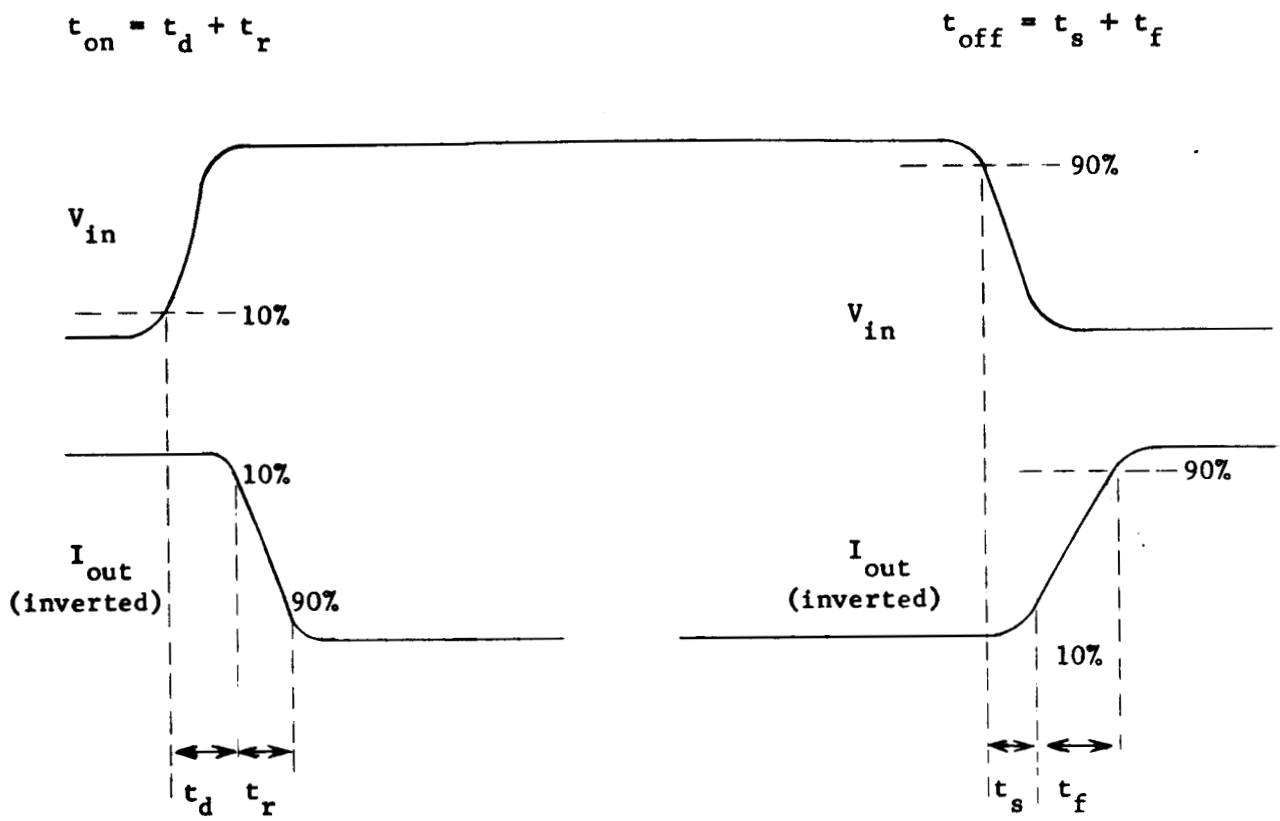


Figure 39

Test Conditions and Typical Display for Switching Test

Test procedure: Device is mounted on appropriate heat sink. $I_{B(on)}$ and $I_{B(off)}$ is measured each test for purpose of adjustment. (I_B in each case may vary with input impedance.) V_{CC} is applied until specific I_C is measured, then switching is measured as described above.

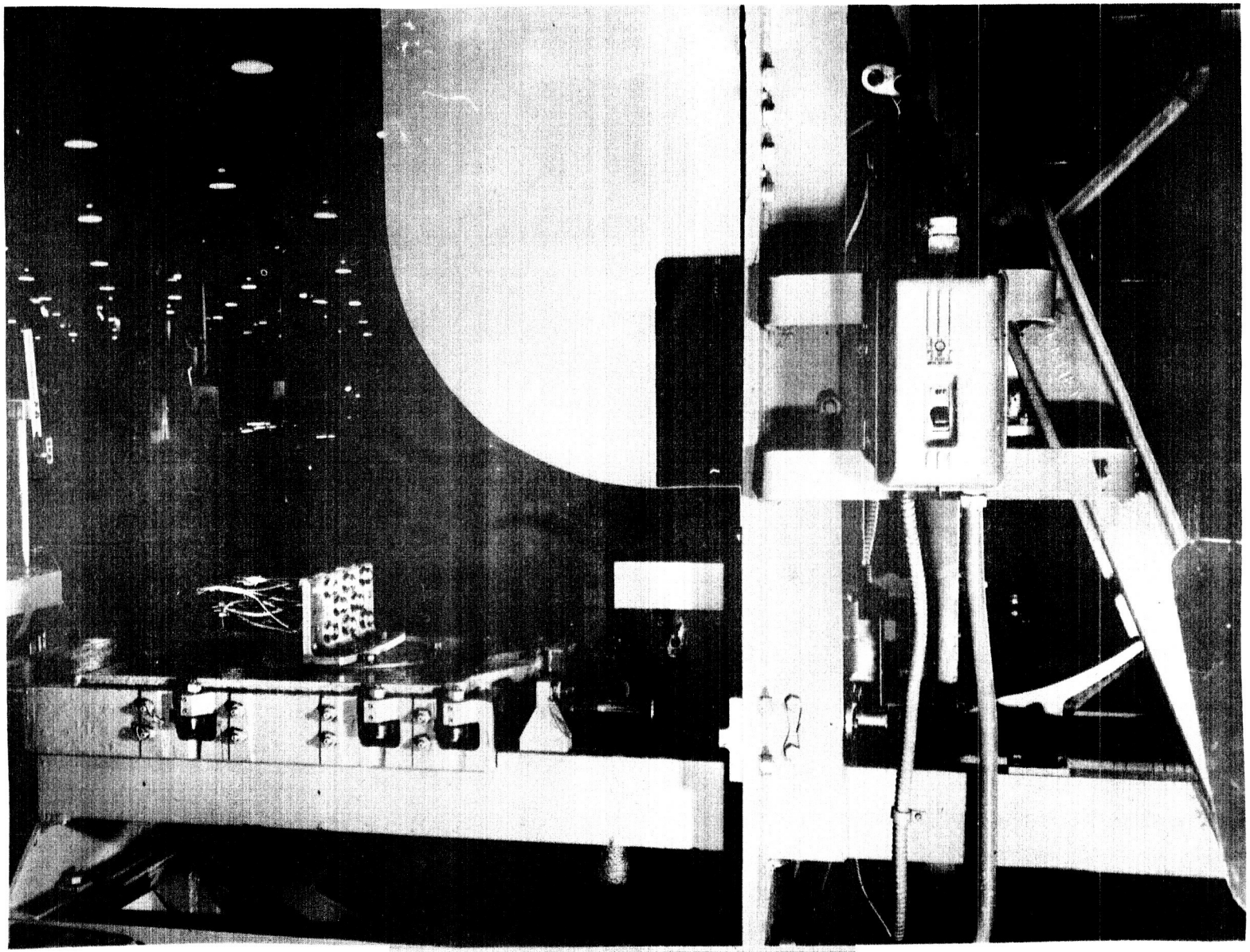


Figure 40

Shock and Centrifuge Test Equipment

Figure 41

Vibration Test Apparatus

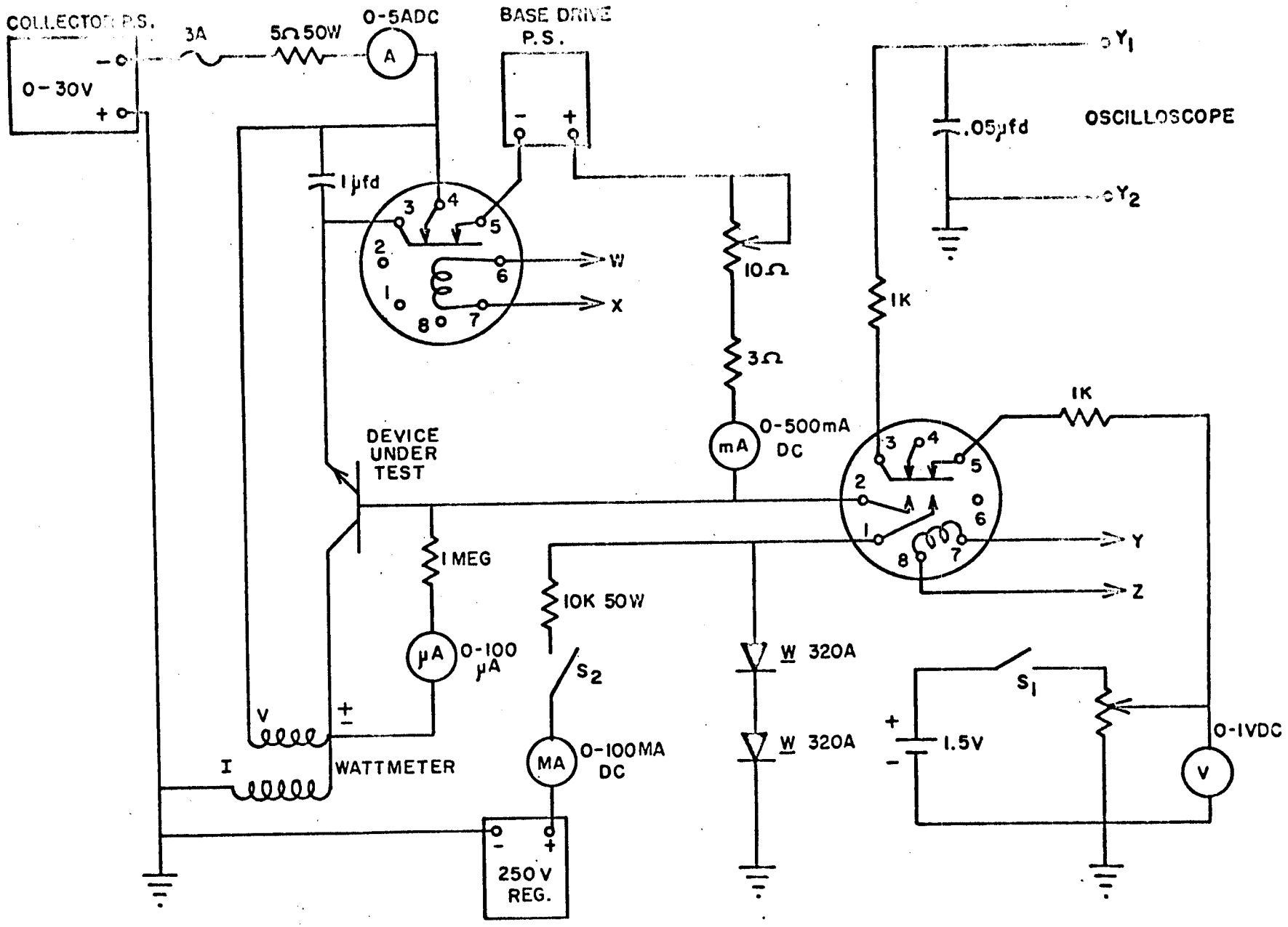


Figure 42

Thermal Test Circuit

VII. CONCLUSIONS AND RECOMMENDATIONS

The success of this project proved that Westinghouse leads the semiconductor industry in the precise control of equipment, materials and processing. It demonstrated the feasibility of fabricating high voltage, high current and high speed devices in large area epitaxial slices. This was accomplished on a small scale, engineering level; it now remains to establish the processes for the large scale production of such a device.

More specific recommendations include:

1. A program to test the device's secondary breakdown.
2. A special circuit should be designed to test switching characteristics at current levels up to 100 amperes.
3. A transistor with the same characteristics as the subject device should be fabricated using a single-diffused design and a comparison made between this and the epitaxial design used here.

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